



H81H3-LM

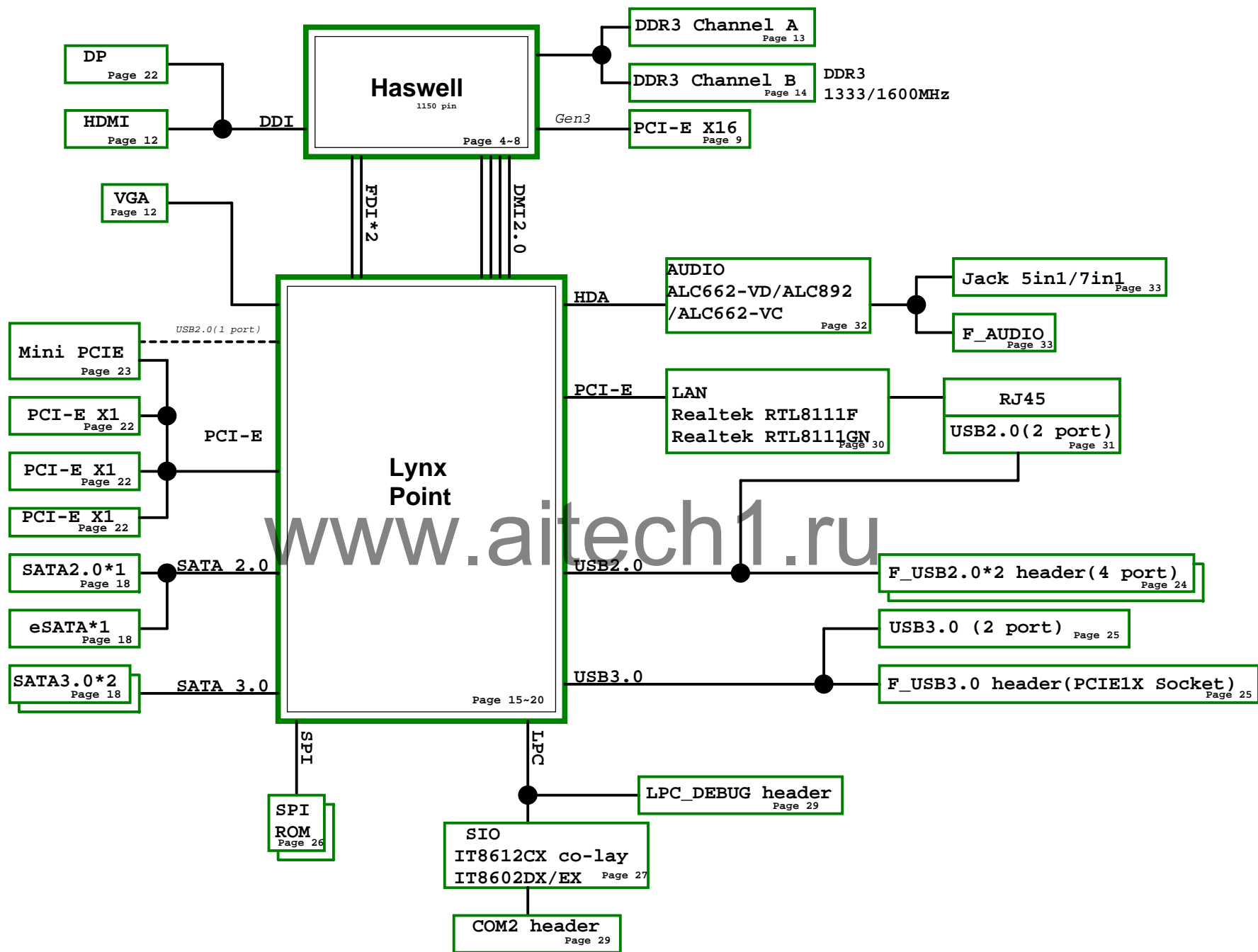
Shark Bay

Rev:1.0
IPG

ECS
CONFIDENTIAL

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PCH-GPIO function

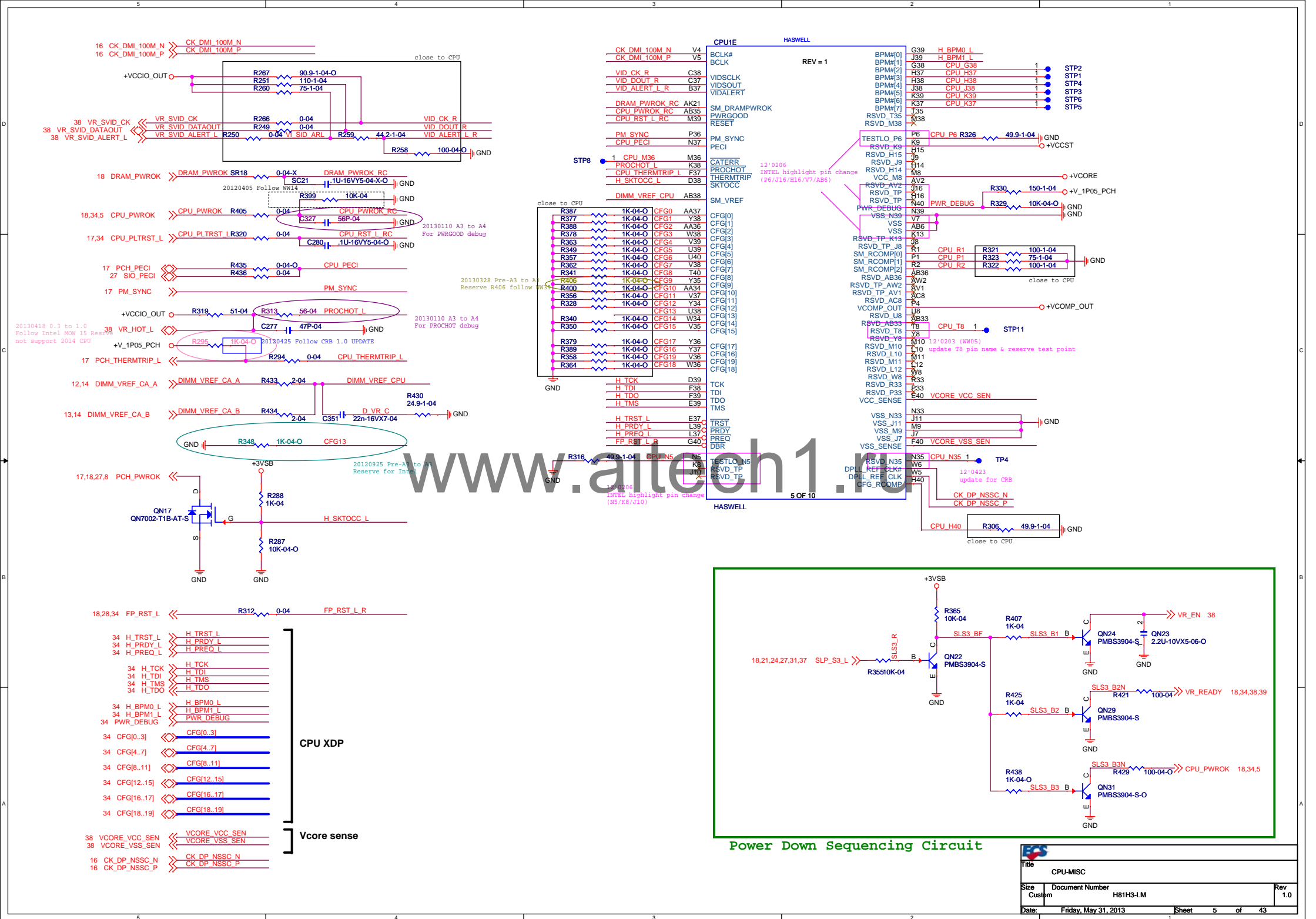
Pin Name	Power Well	Usage	Default Status	Boot Set
GPIO13	3VSB	PCH_GPIO13 (USB Charger CTL1)	GPI	GPO
GPIO14	3VSB	TS_F	OC7#	GPI
GPIO15	3VSB	PCIE16X_RST_L	GPO	GPI
GPIO22	VCC3	SW_CLR_CMOS	GPI	GPI
GPIO24	3VSB	ME disable	GPO	GPO
GPIO25	3VSB	PCH_GPIO25 (USB Charger CTL3)	PCIECLKRQ3#	GPO
GPIO26	3VSB	PCH_GPIO26 (USB Charger CTL4)	PCIECLKRQ4#	GPO
GPIO27	+ATX_3VSB	MS_GP0(Mode_Switch)	GPO	GPI
GPIO28	+ATX_3VSB	MS_GP1(Mode_Switch)	GPO	GPI
GPIO29	3VSB	PCH_GPIO29(BOM detect)	GPI	GPI
GPIO31	3VSB	PCH_GPIO31(+VDIMM select)	GPI	GPO
GPIO39	VCC3	CAS0(SEN_HEADER)	GPI	GPI
GPIO45	3VSB	LAN_DIS_L(MINI_PCIE)	PCIECLKRQ6#	GPO
GPIO48	VCC3	CAS1(SEN_HEADER)	GPI	GPI
GPIO49	VCC3	PCH_GPIO49 USB/PCIE(mSATA) DET	GPI	GPO
GPIO50	VCC3	PS2_DET	GPI	GPI
GPIO52	VCC3	PCH_GPIO52 (FP_AUD_DETECT)	GPI	GPO
GPIO54	VCC3	COM_DET	GPI	GPI
GPIO57	3VSB	MODE_CTRL(Mode_Switch)	GPI	GPI
GPIO60	3VSB	PCH_GPIO60(BOM detect)	SML0ALERT#	GPI
GPIO64	VCC3	PCH_GPIO64(BOM detect)	CLKOUTFLEX0	GPI
GPIO65	VCC3	PCH_GPIO65(BOM detect)	CLKOUTFLEX1	GPI
GPIO66	VCC3	PCH_GPIO66(BOM detect)	CLKOUTFLEX2	GPI
GPIO73	3VSB	PCH_GPIO73	PCIECLKRQ0#	GPI
GPIO74	3VSB	PCH_GPIO74(BOM detect)	SML1ALERT#	GPI

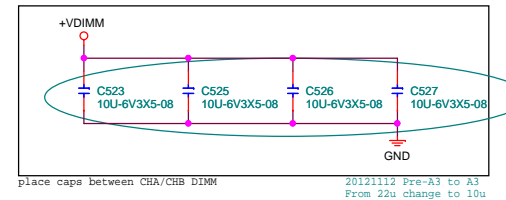
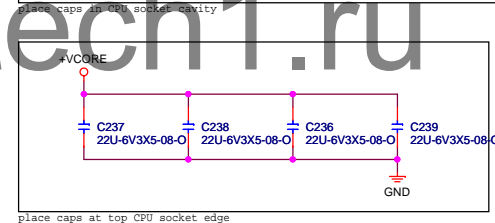
SIO-GPIO function

Pin Name	Power Well	Usage	Default SET
GP12	VCC3	PCIRST1_L	GPO
GP22	3VSB	SIO_LED0	GPIO
GP43	3VSB	SIO_LED1	GPIO
GP56	VCC3	TS_F	GPIO

Interrupt mapping

Function	INT# port	PCle*1 port	Device
LAN	INTC#	port 3	RTL8111GN
PCIE1X_1	INTB#	port 2	LPT integrate
PCIE1X_2	INTD#	port 4	LPT integrate
PCIE1X_3	INTA#	port 5	LPT integrate
mini-PCIE	INTB#	port 6	LPT integrate
SATA	INTB#	N/A	LPT integrate





PCIE SPEC

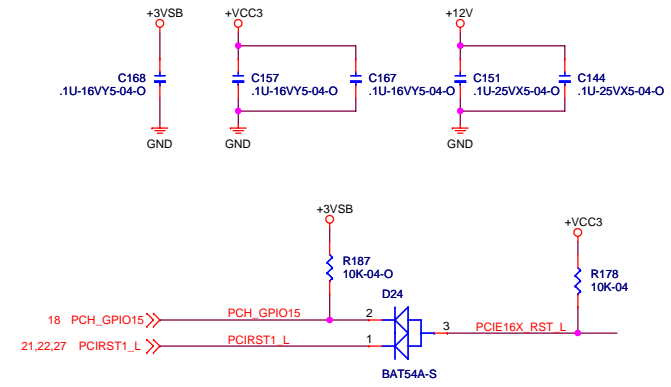
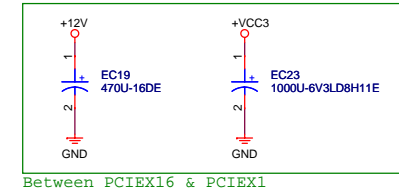
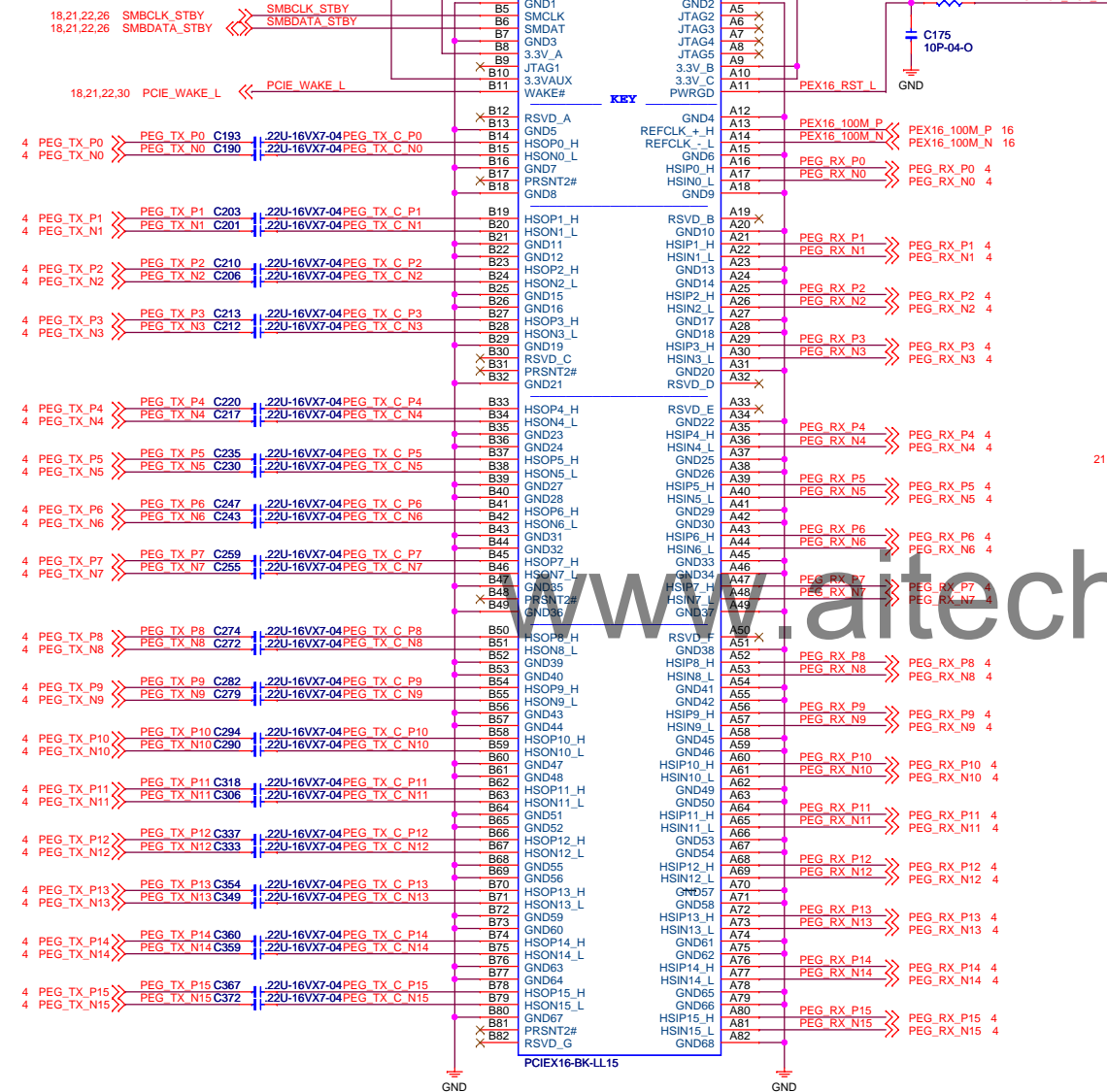
VCC3: 3A

12V: 5.5A

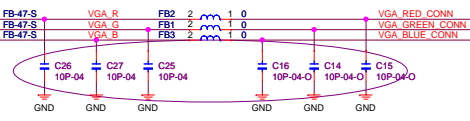
3VSB: 0.375A

20130411 A4 to A5
Change Name for Lenovo spec

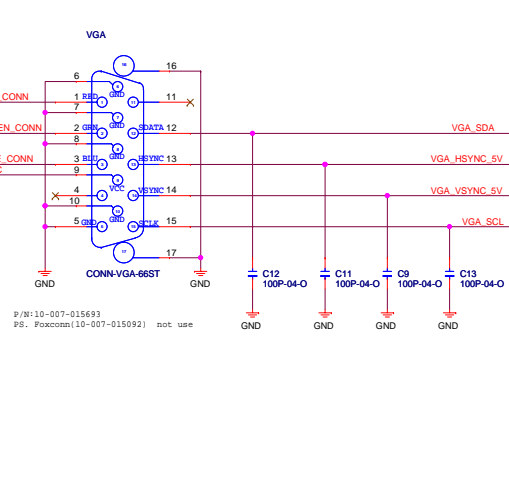
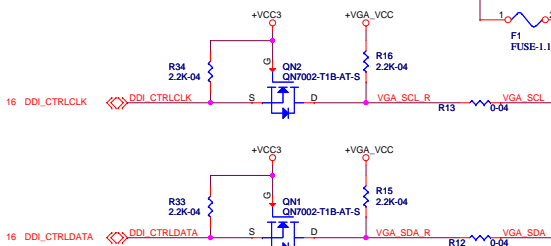
20130322 A4 to A5
Change to GND



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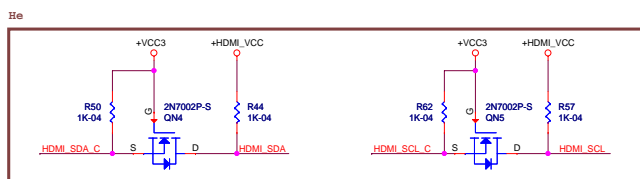
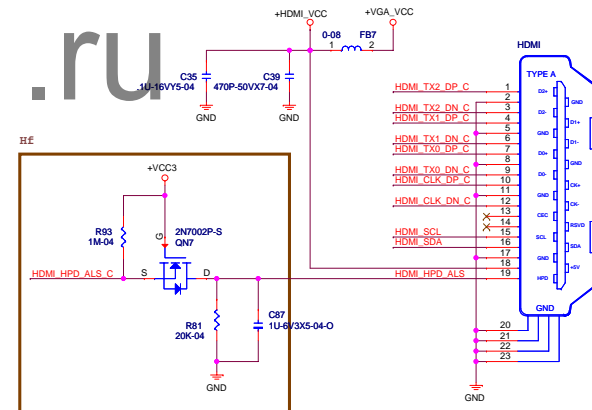
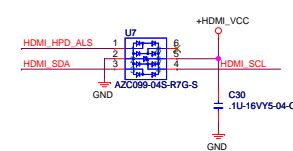
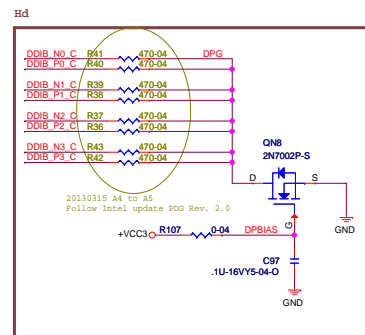
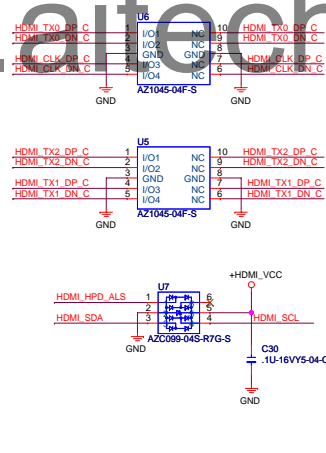
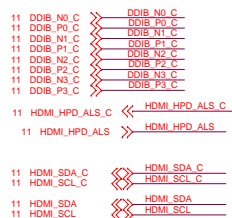
20121212 A3 to A4
Change vaule for VGA Debug



P/N:10-007-015693

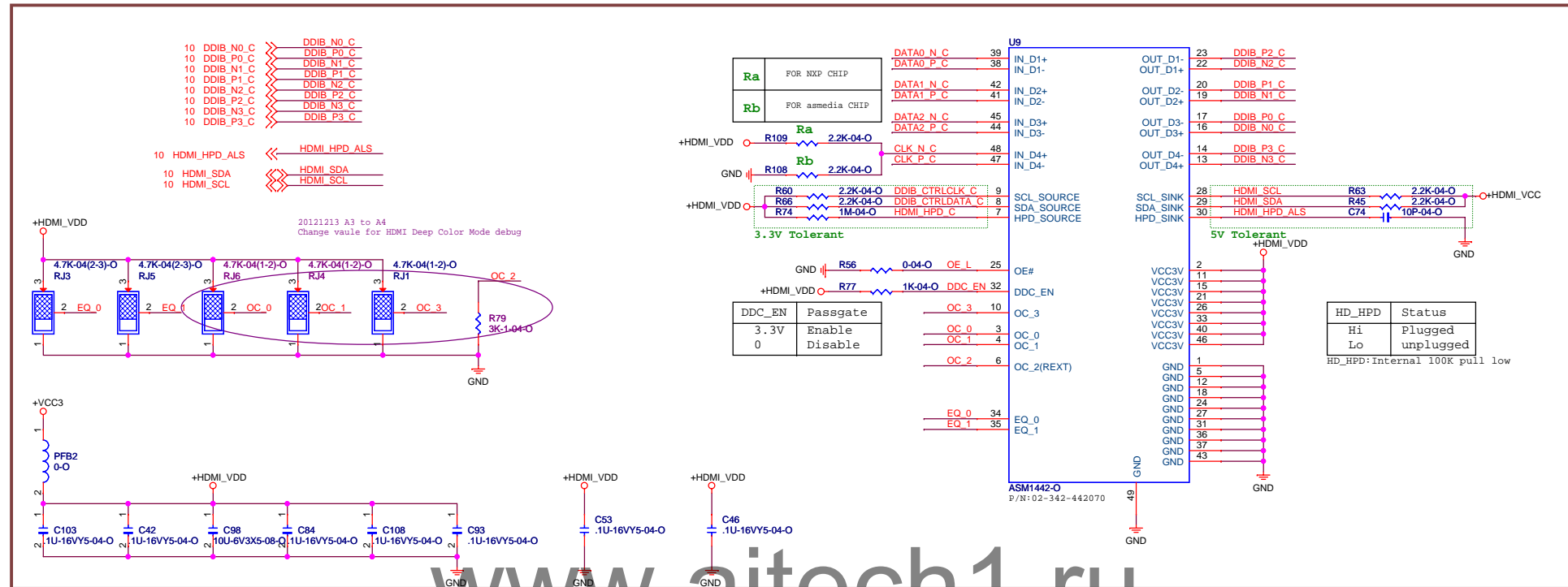
PS. Foxconn(10-007

HDMI

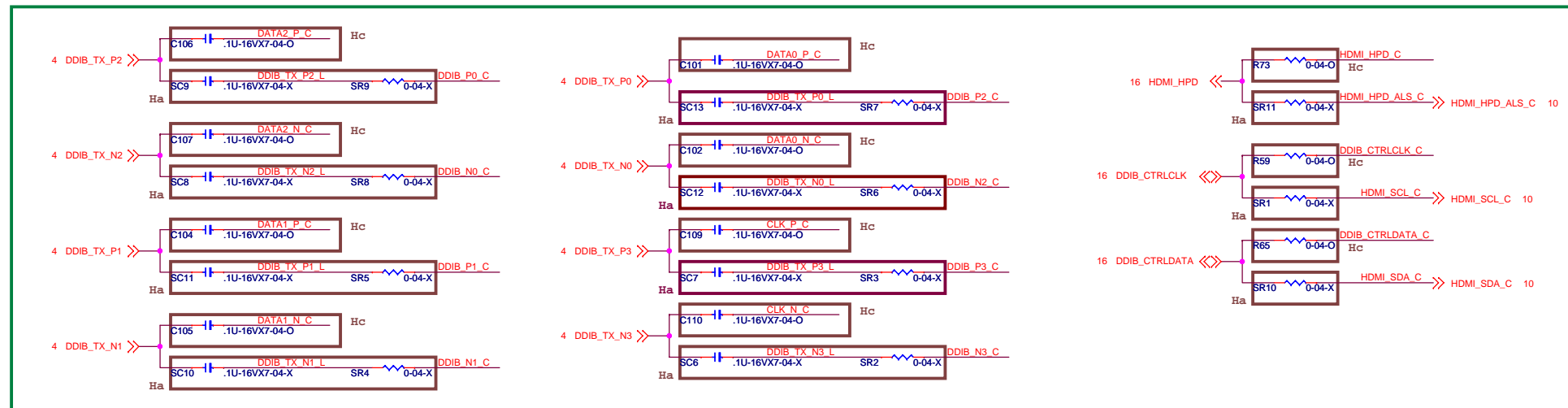


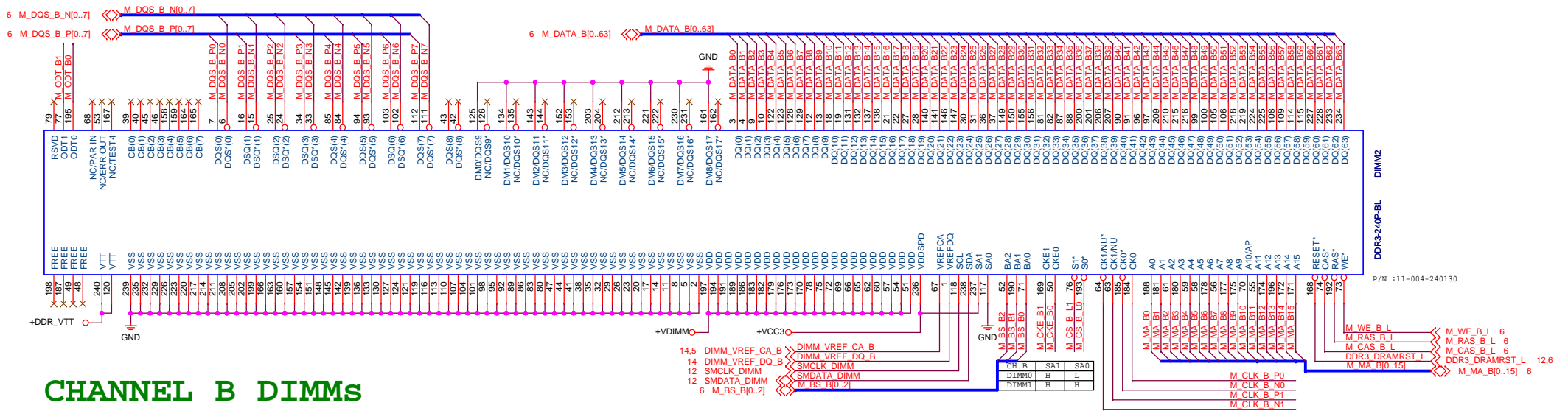
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Level Shift	X	V	V	X	X	X
Non Level shift	V	X	X	V	V	V

Hb

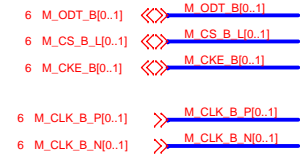


HDMI Signal Option Close (Level shift)ASM1442





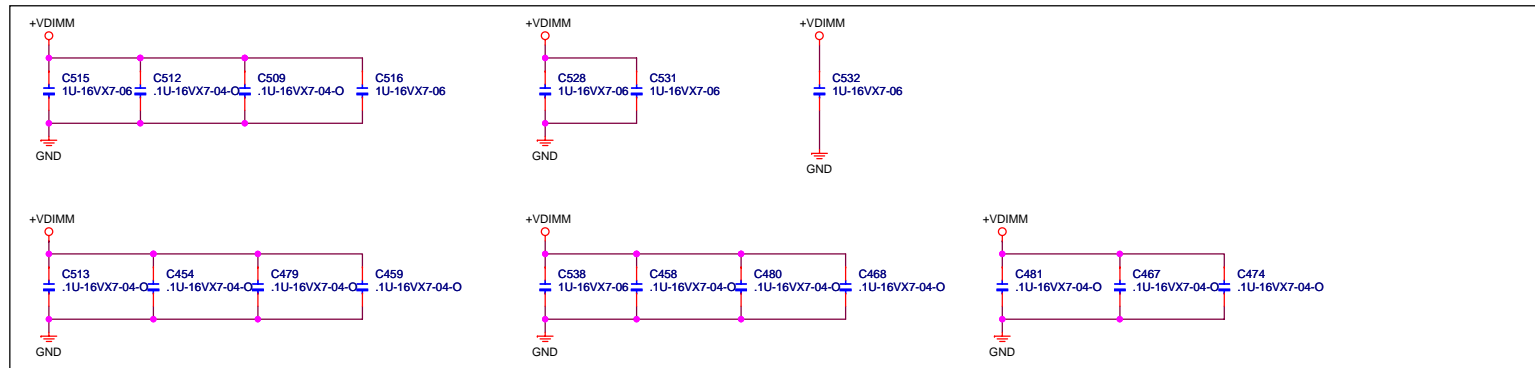
CHANNEL B DIMMs



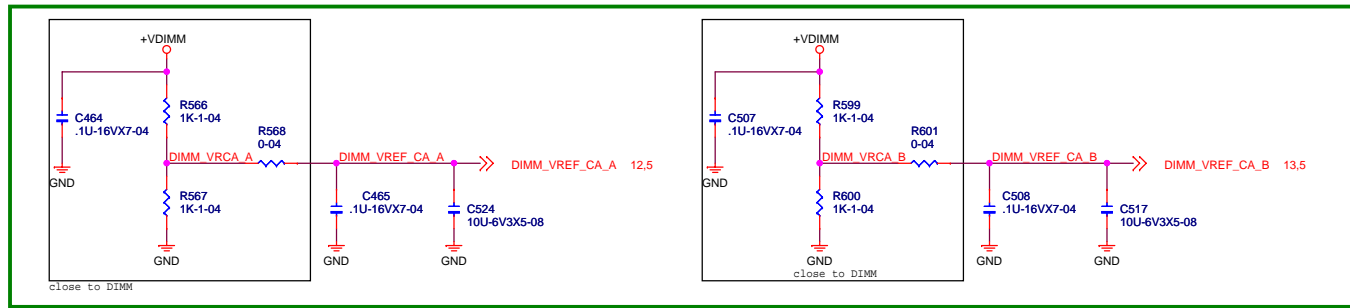
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close to CHB-DIMM0

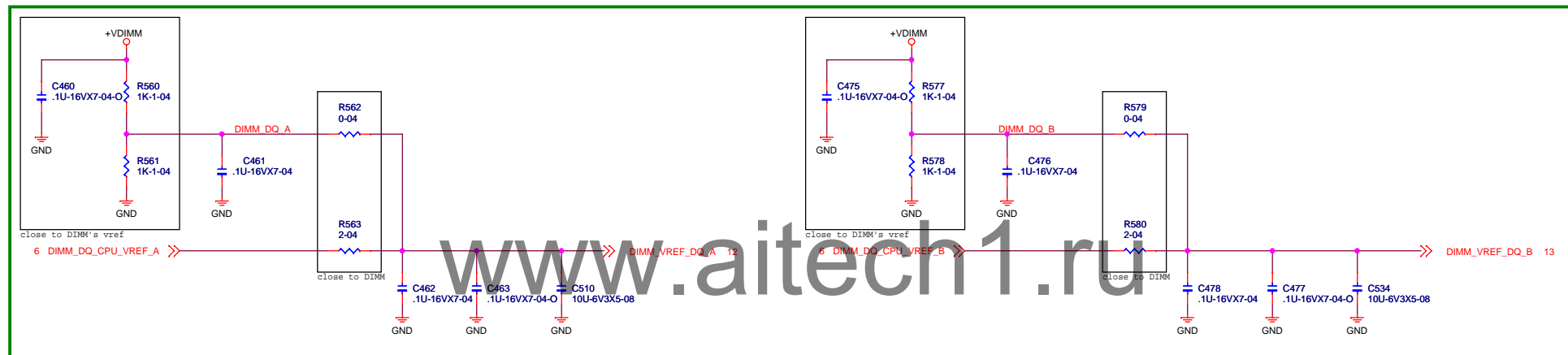
close to CHB-DIMM0



stitching caps for CMD,CTL,ADDR

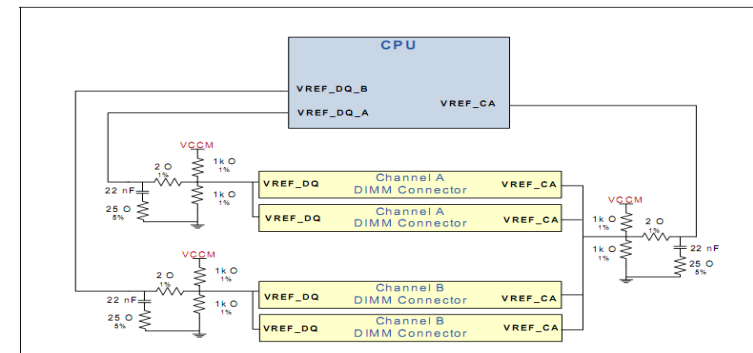


DIMM_VREF_CA Circuit

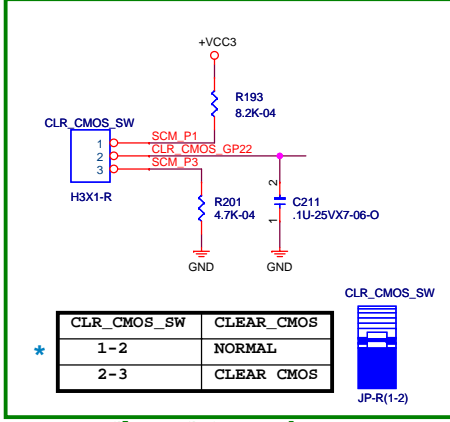
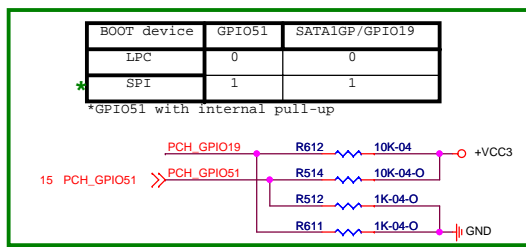
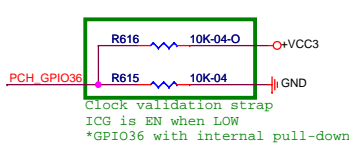
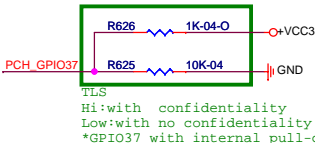
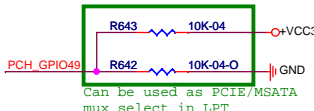
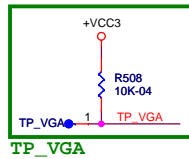
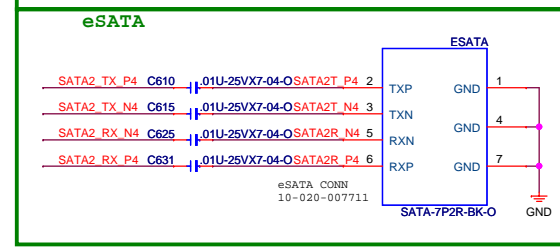
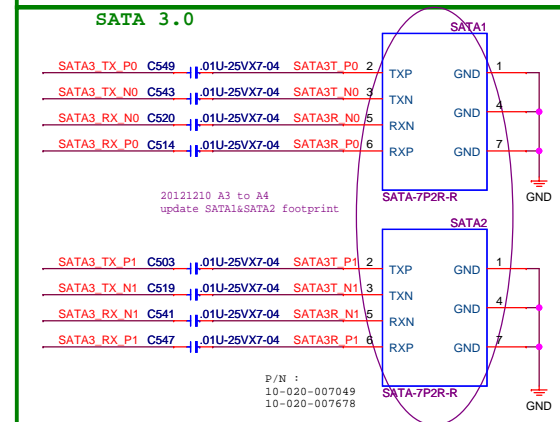
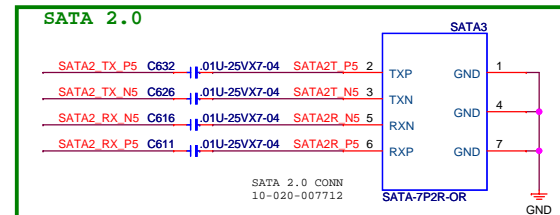
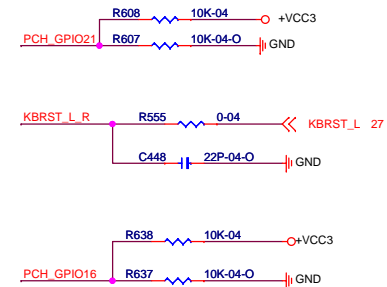
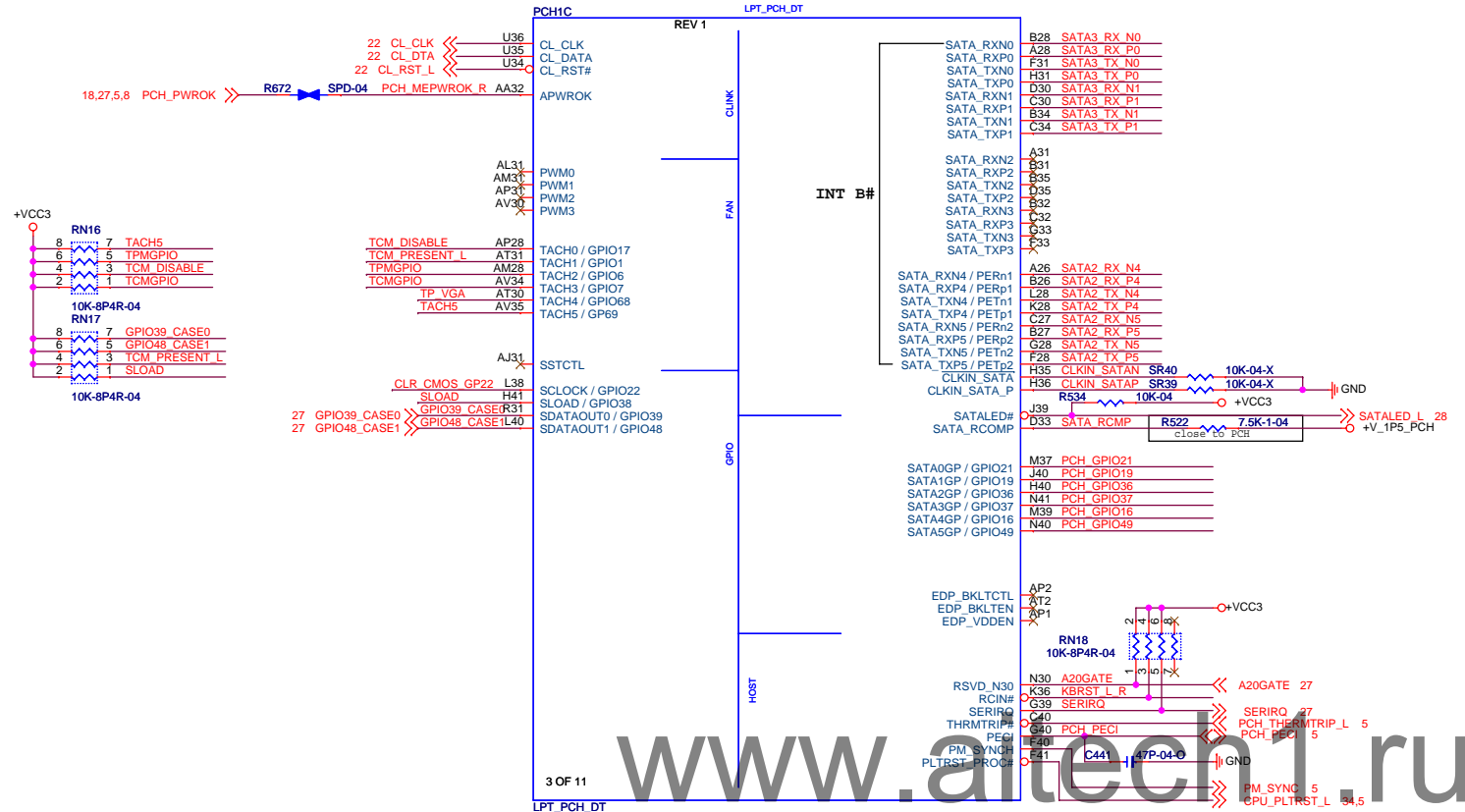


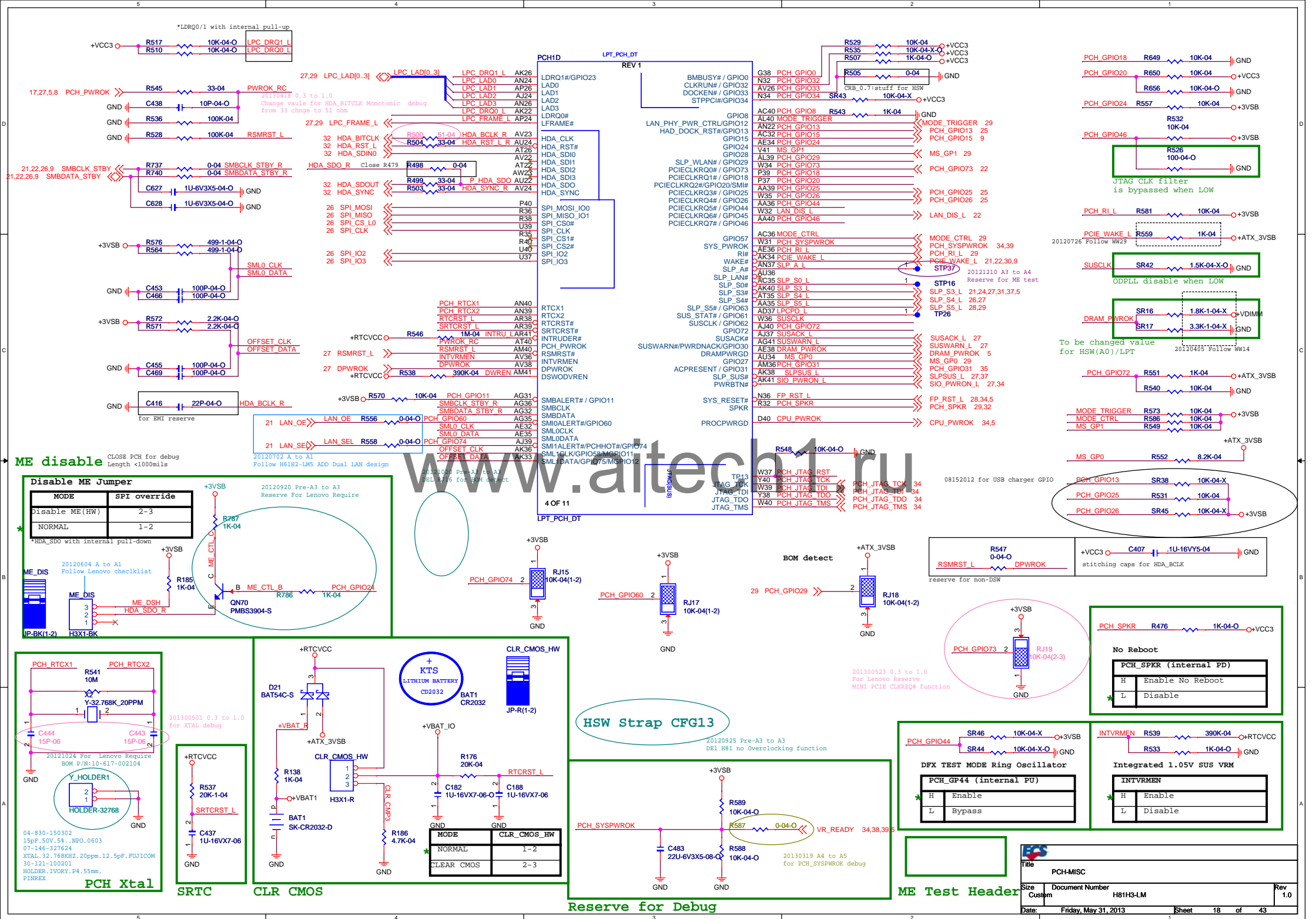
DIMM_VREF_DQ Circuit

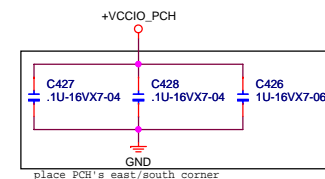
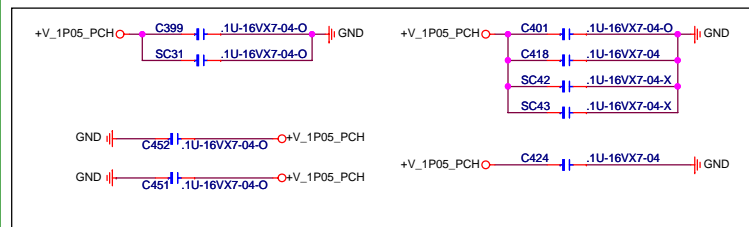
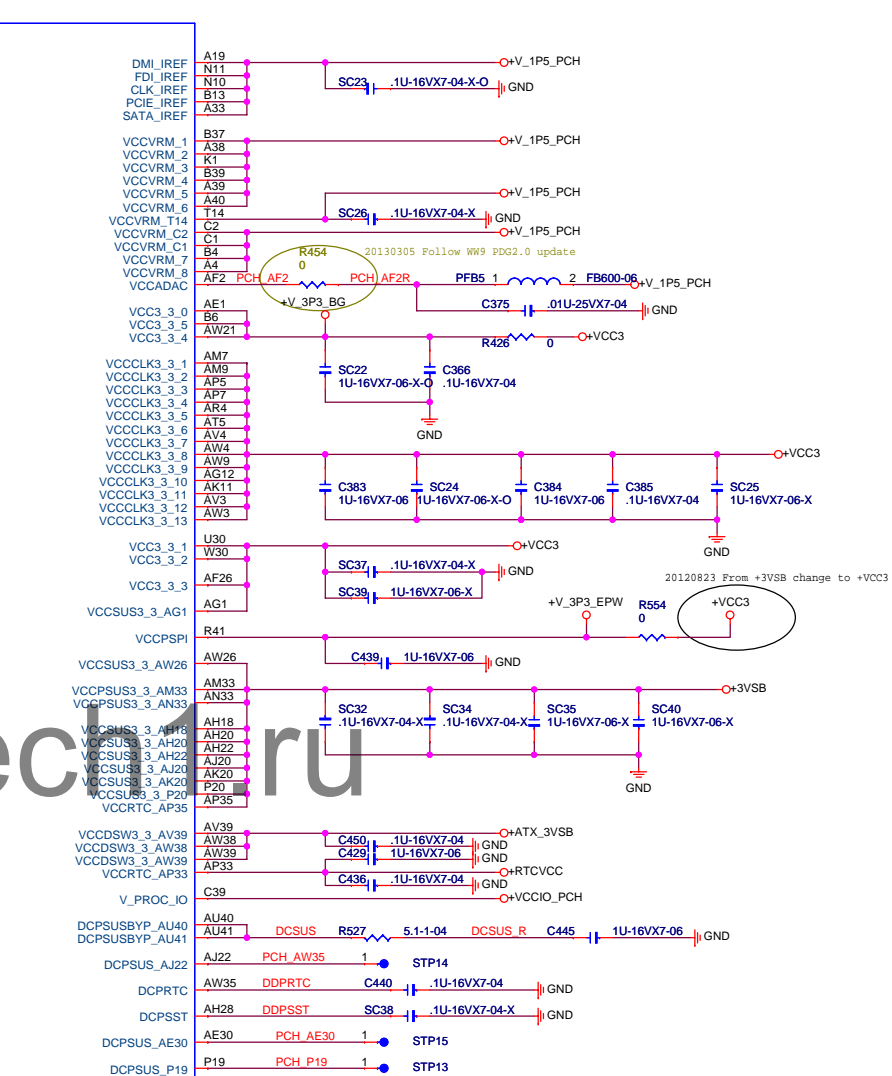
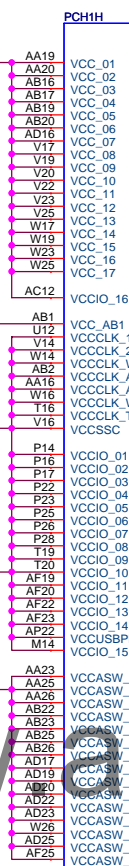
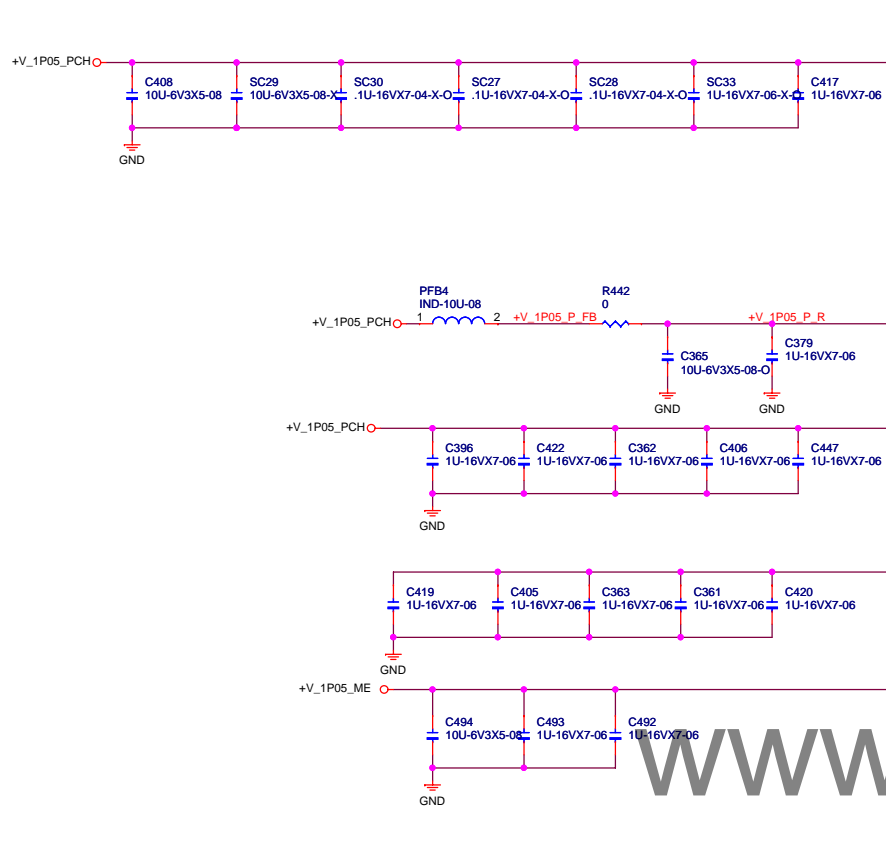
Figure 4-8. DDR3 VREF Topologies



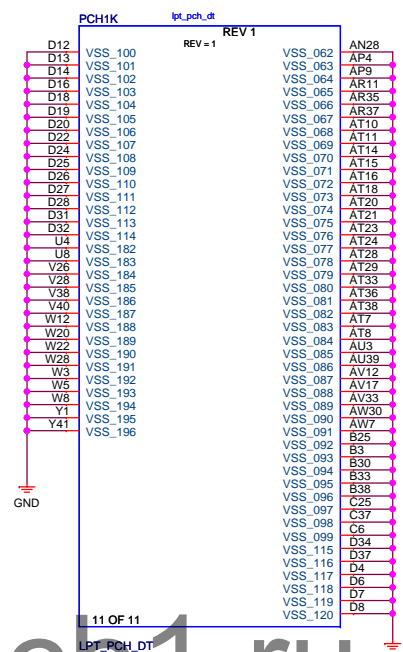
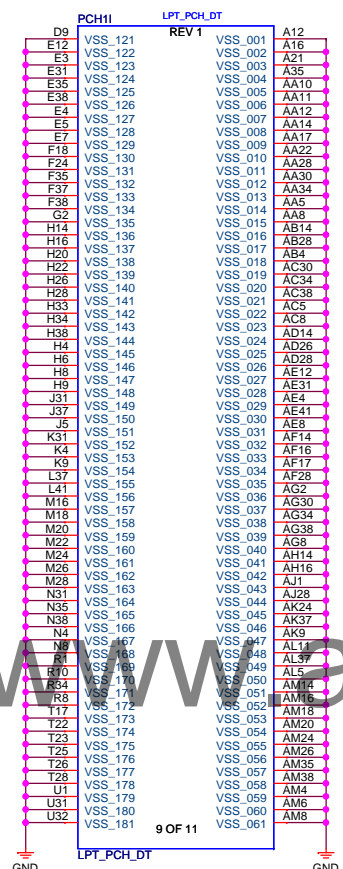
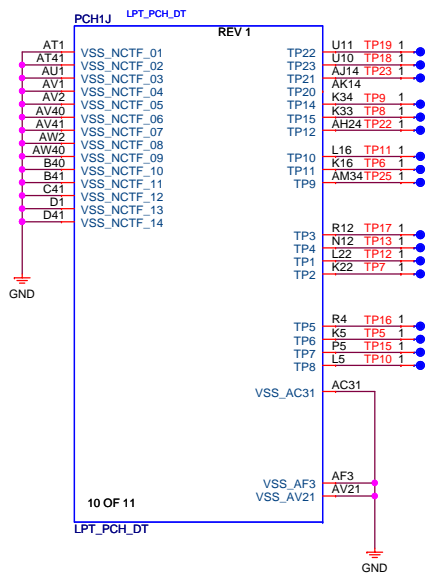
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PCH-POWER			
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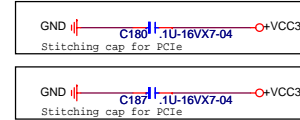
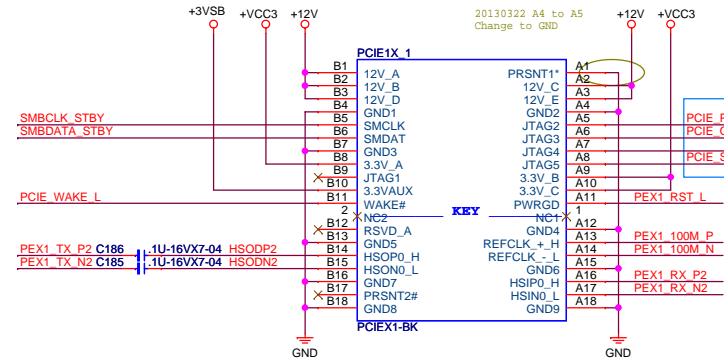
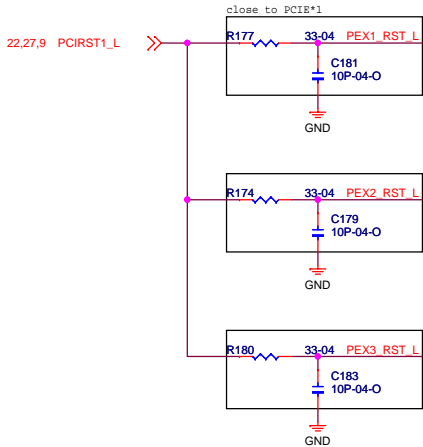
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18,22,26,9 SMBDATA_STBY >> SMBDATA_STBY
18,22,30,9 PCIE_WAKE_L >> PCIE_WAKE_L

16 PEX1_100M_P >> PEX1_100M_P
16 PEX1_100M_N >> PEX1_100M_N
16 PEX2_100M_P >> PEX2_100M_P
16 PEX2_100M_N >> PEX2_100M_N
16 PEX3_100M_P >> PEX3_100M_P
16 PEX3_100M_N >> PEX3_100M_N

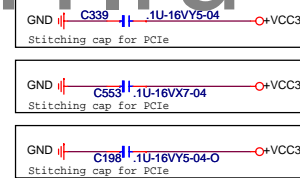
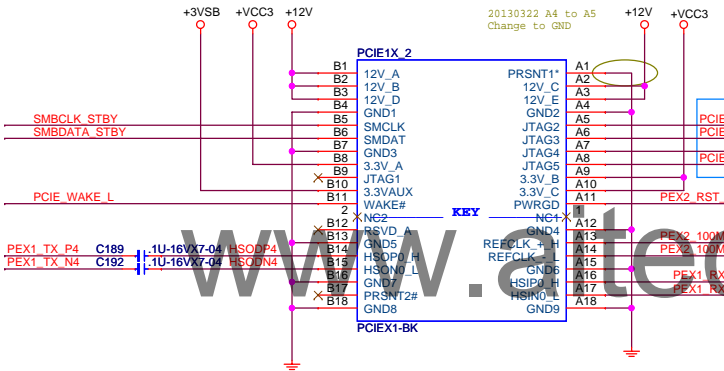
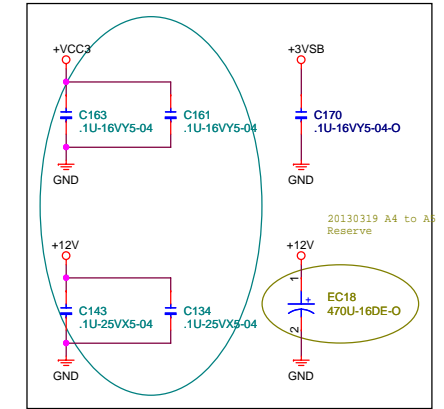
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15 PEX1_TX_N2 >> PEX1_TX_N2
15 PEX1_RX_P2 >> PEX1_RX_P2
15 PEX1_RX_N2 >> PEX1_RX_N2

15 PEX1_TX_P4 >> PEX1_TX_P4
15 PEX1_TX_N4 >> PEX1_TX_N4
15 PEX1_RX_P4 >> PEX1_RX_P4
15 PEX1_RX_N4 >> PEX1_RX_N4

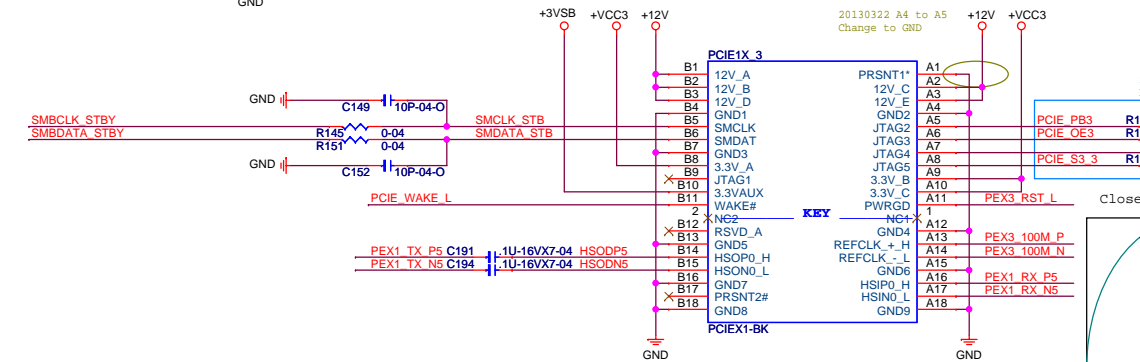
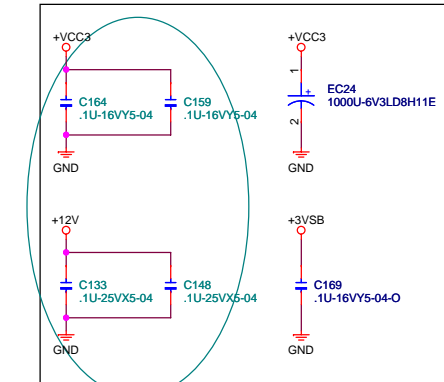
15 PEX1_TX_P5 >> PEX1_TX_P5
15 PEX1_TX_N5 >> PEX1_TX_N5
15 PEX1_RX_P5 >> PEX1_RX_P5
15 PEX1_RX_N5 >> PEX1_RX_N5



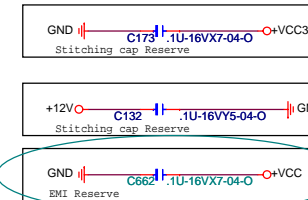
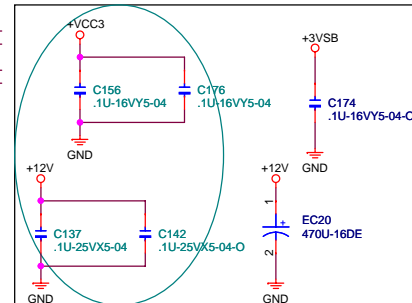
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Close PCIE1X 2 Slot

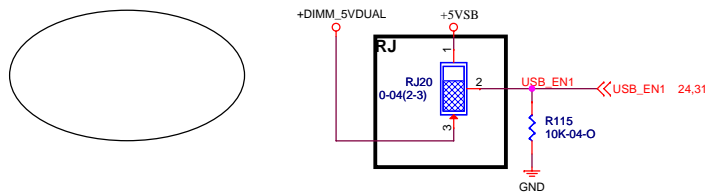


Close PCIE1X 3 Slot



Title				PCIE1X*3
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	uP7550 Enable use	RJ	S4/S5 USB_5V_DUAL	
*	+DIMM_5VDUAL	0ohm (2-3)	0 Volt	Lenovo S4/S5 w/o USB_5V_DUAL
	5VSB	0ohm (1-2)	5 Volt	

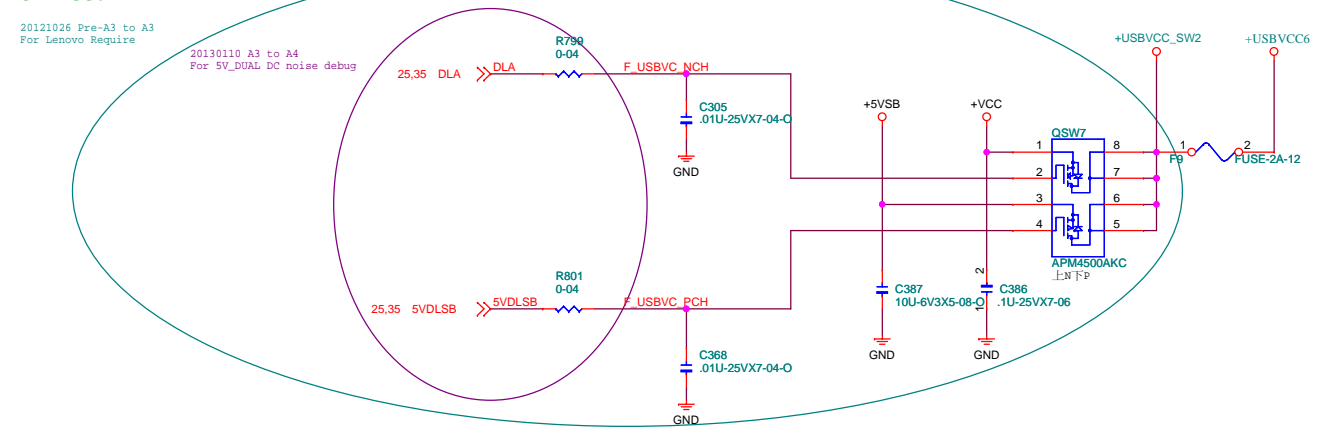


20120810 for Lenovo request

+USBVCC6

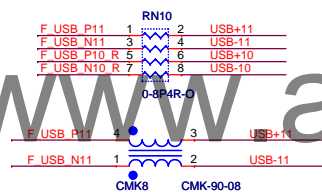
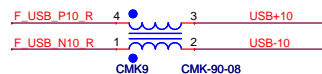
20121026 Pre-A3 to A3
For Lenovo Require

20130110 A3 to A4
For 5V_DUAL DC noise debug

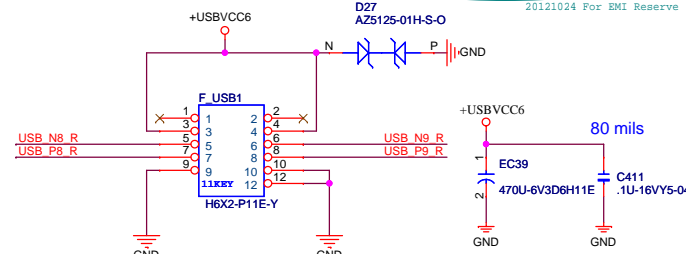
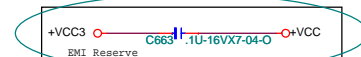
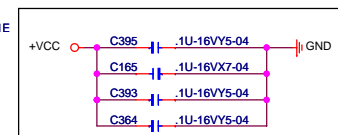
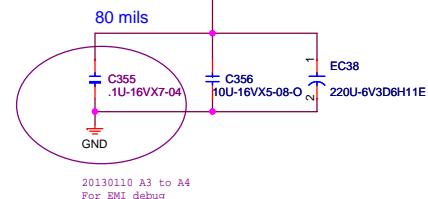
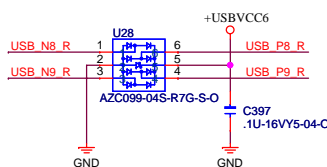
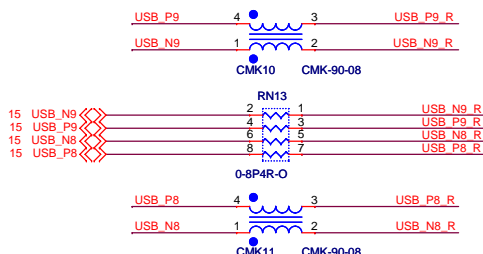
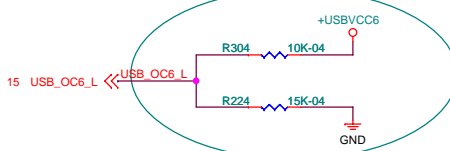


USB2.0 header

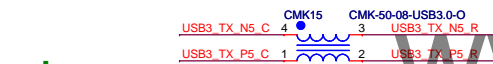
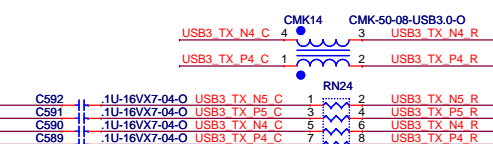
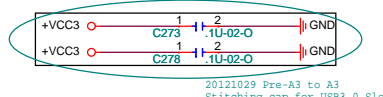
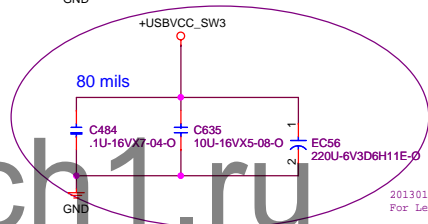
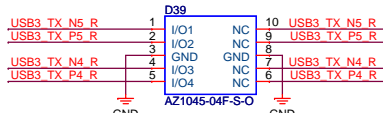
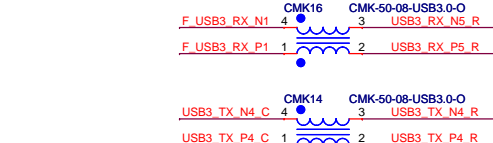
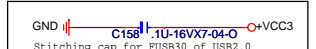
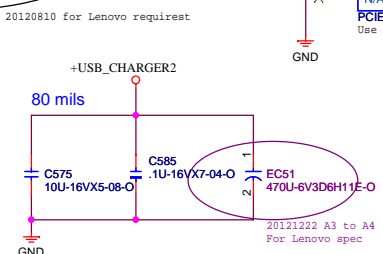
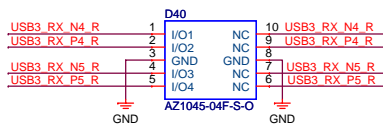
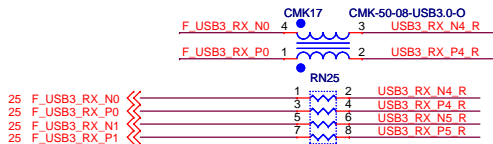
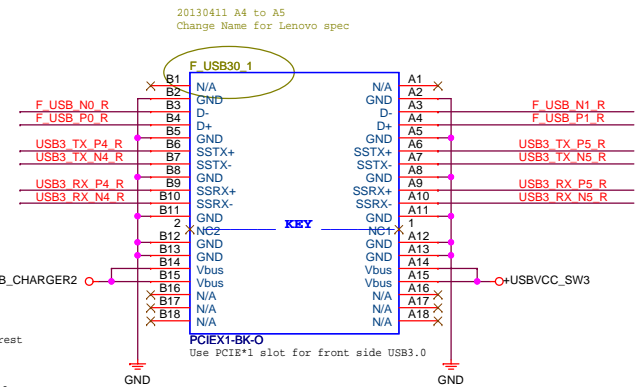
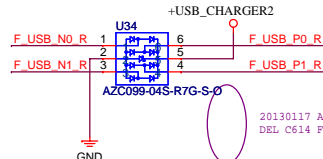
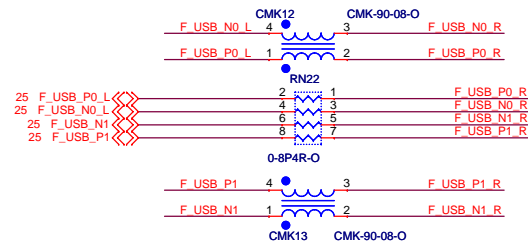
- 25 F_USB_N10_R
- 25 F_USB_P10_R
- 25 F_USB_P11
- 25 F_USB_N11



20121029 Pre-A3 to A3
For Lenovo Require



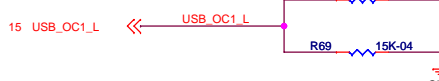
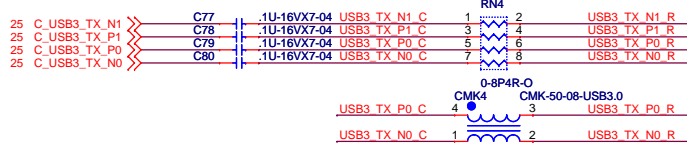
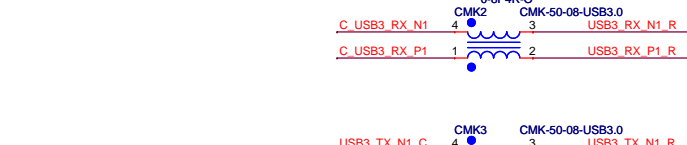
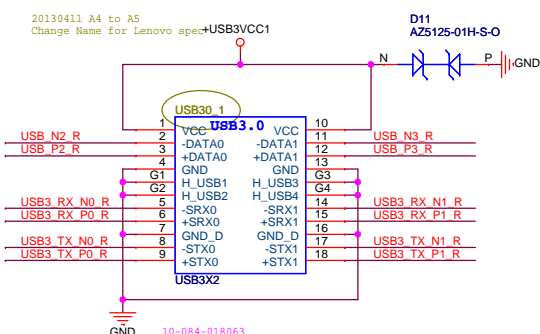
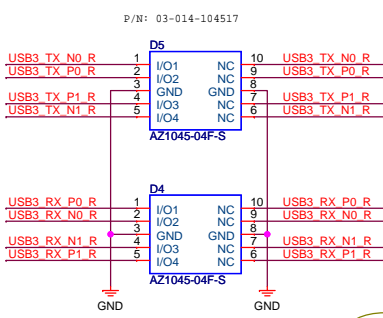
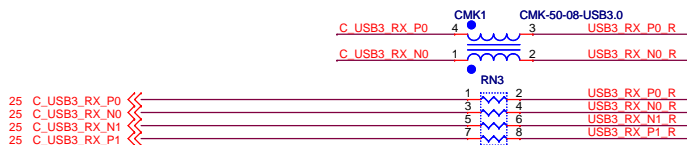
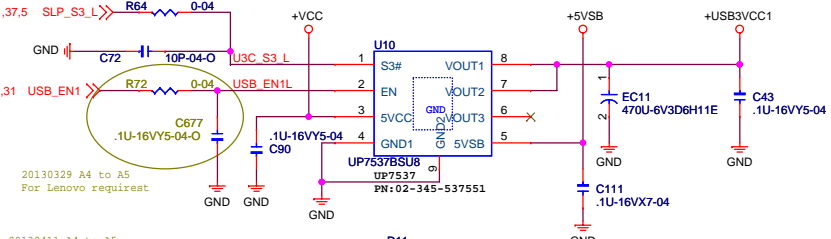
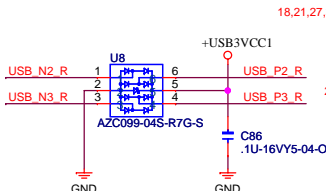
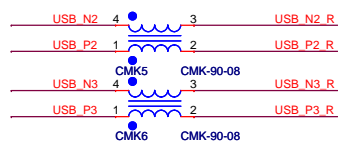
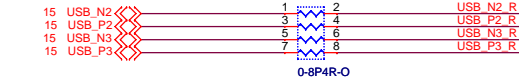
Title USB2.0 Header		
Size Custom	Document Number H81H3-LM	Rev 1.0
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USB3.0 slot

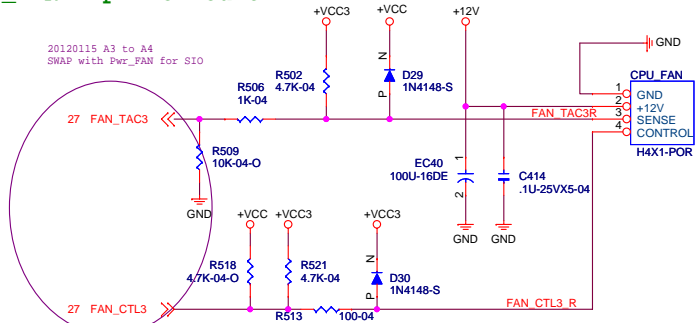
USB3.0 connector

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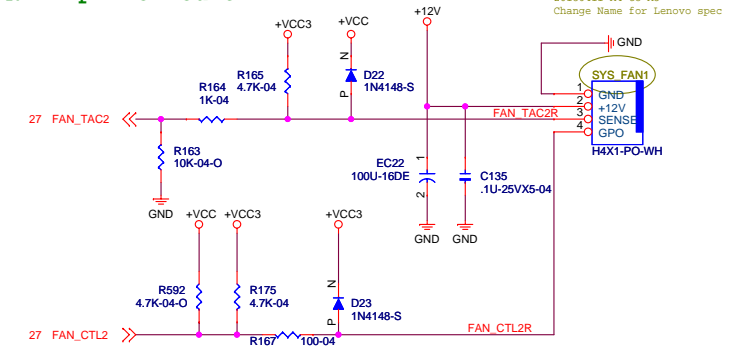


Title			USB3.0 Conn & Slot
Size	Document Number	H81H3-LM	
Custom			
Date:	Friday, May 31, 2013	Sheet	24 of 43

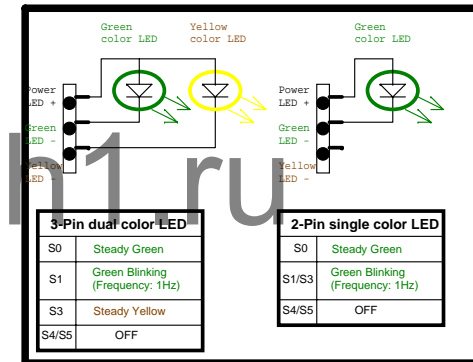
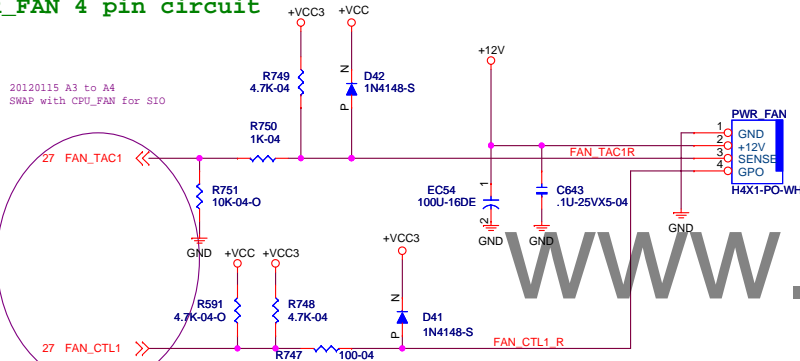
CPU_FAN 4 pin circuit



SYS_FAN1 4 pin circuit



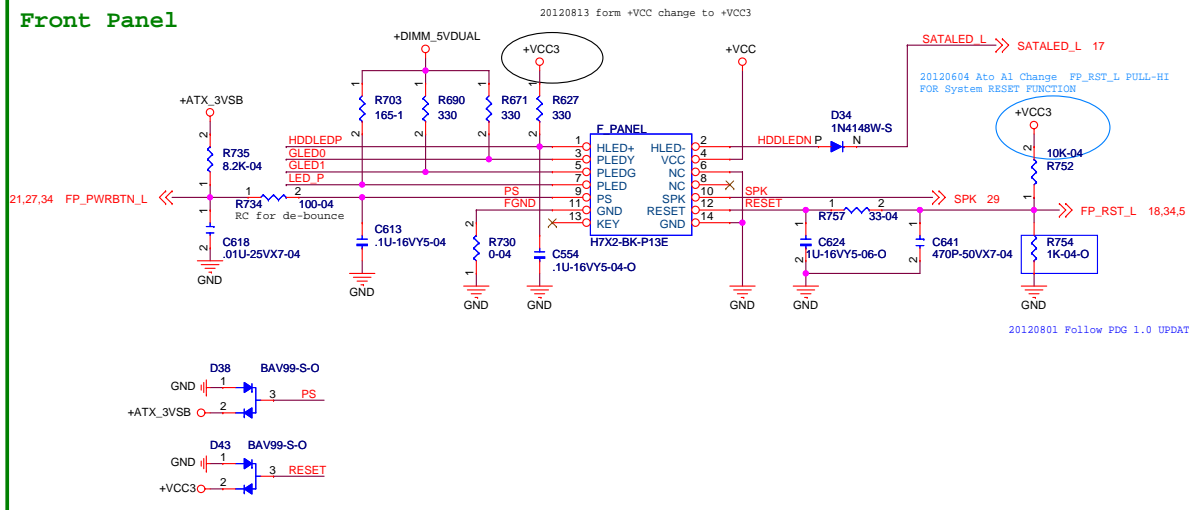
PWR_FAN 4 pin circuit



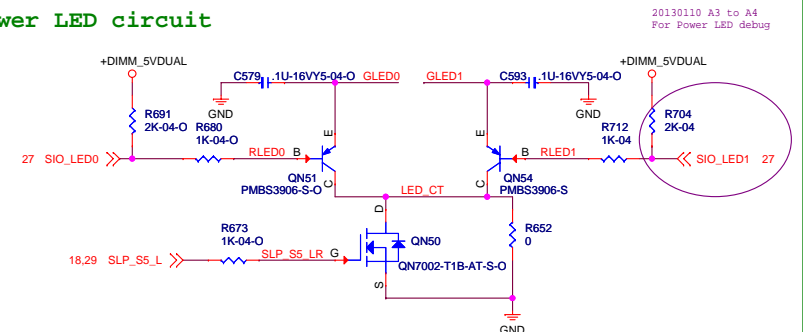
Lenovo LED線路阻値330-06

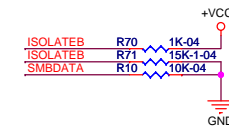
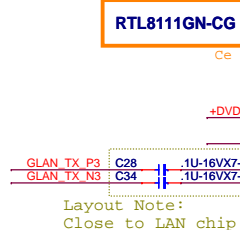
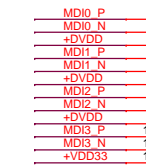
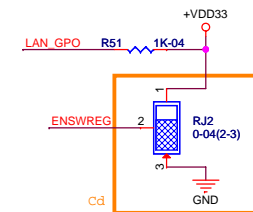
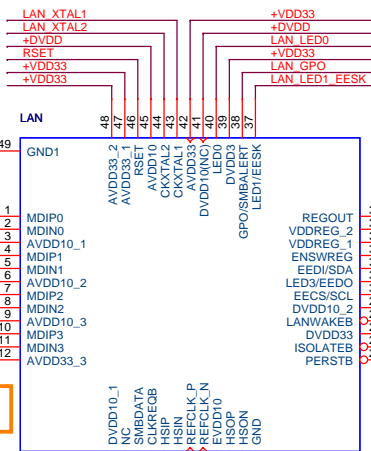
Source Voltage (V)	5
LED Forward Voltage (V)	1.8
BIT Vce(s) (V)	0
Pull Up Resistor (ohm)	330
LED Forward Current (A)	0.009697
Pull Up Resistor Power (R<1/10 W)	0.03103
LED Power (W)	0.017455

Front Panel

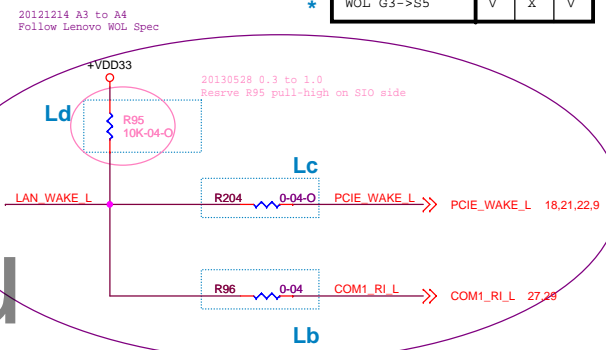


Power LED circuit



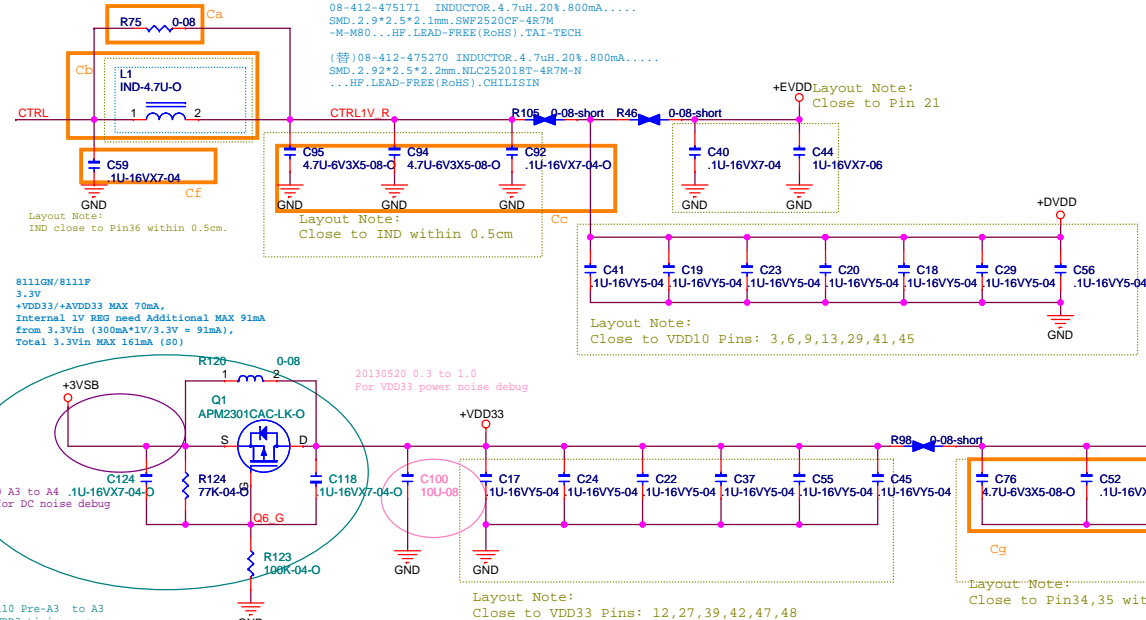
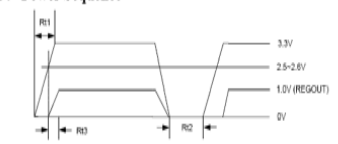
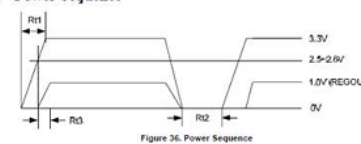


MODE	Lb	Lc	Ld
WOL Normal	X	V	X
WOL G3->S5	V	X	V




Chip/version	1.0V/1.05	Ca	Cb	Cc	Cd	Ce	Cf	Cg
RTL8111GN-CG 01-267-111366	LDO	V	X	X	RJ2(2-3)	RTL8111GN-CG	V	X
	SWR	X	V	V	RJ2(1-2)	RTL8111GN-CG	X	V
RTL8111F-VB-CG 01-267-111362	SWR	X	V	V	RJ2(1-2)	RTL8111F-VB-CG	X	V

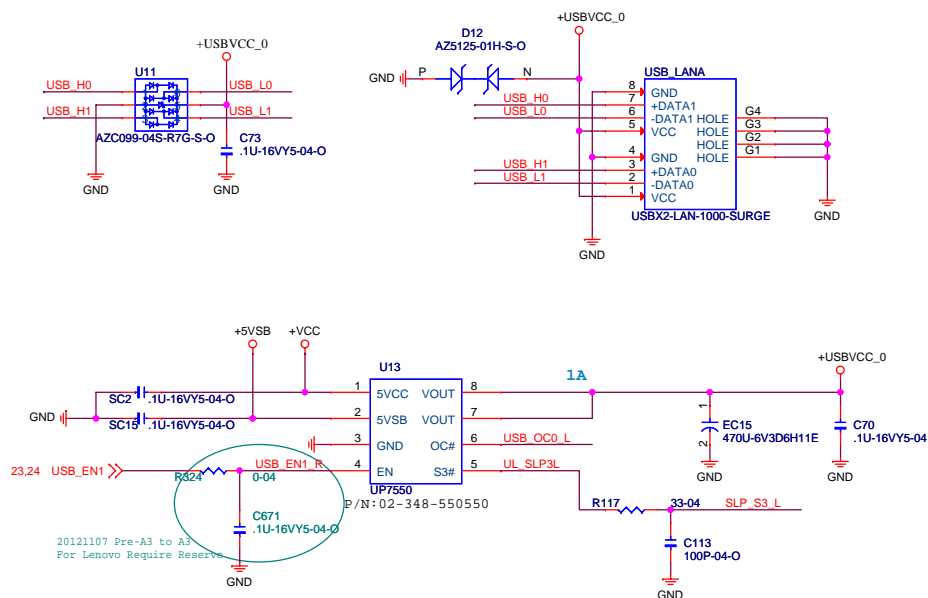
Note: Power Sequence
2012 0815 update



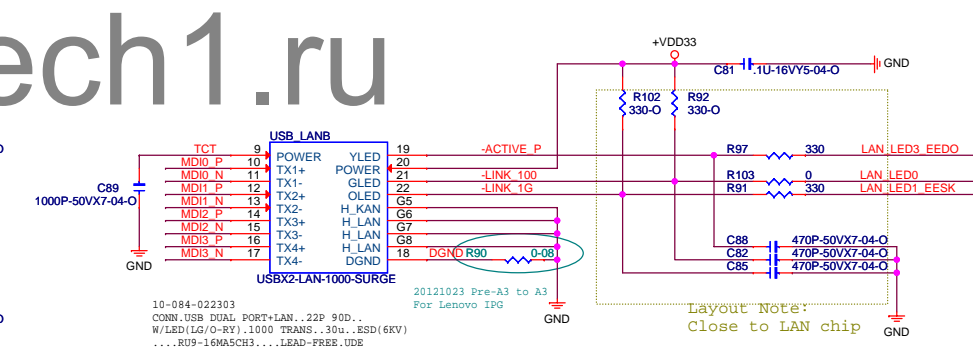
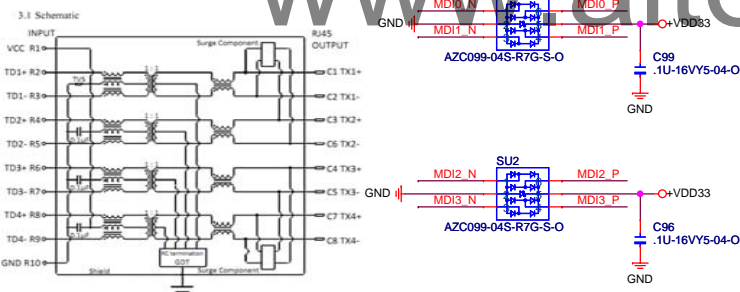
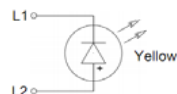
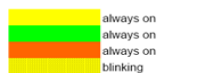
RLT8111GN-CG

RLT8111F-VB-CG

			
Title			
LAN RTL8111GN Colay RTL8111F			
Size	Document Number		Rev
Custom	H81H3-LM		1.0
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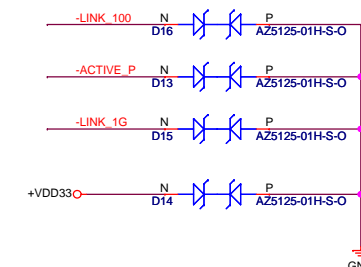
WOL	status	Yellow	Grn/Org
don't care	No Link	off	off
off(ME WOL and Host WOL should be disable both)	S3/S4/S5	off	off
on	10M_inactive		off
on	10M_active		off
on	100M_inactive		
on	100M_active		
on	1G_inactive		
on	1G_active		



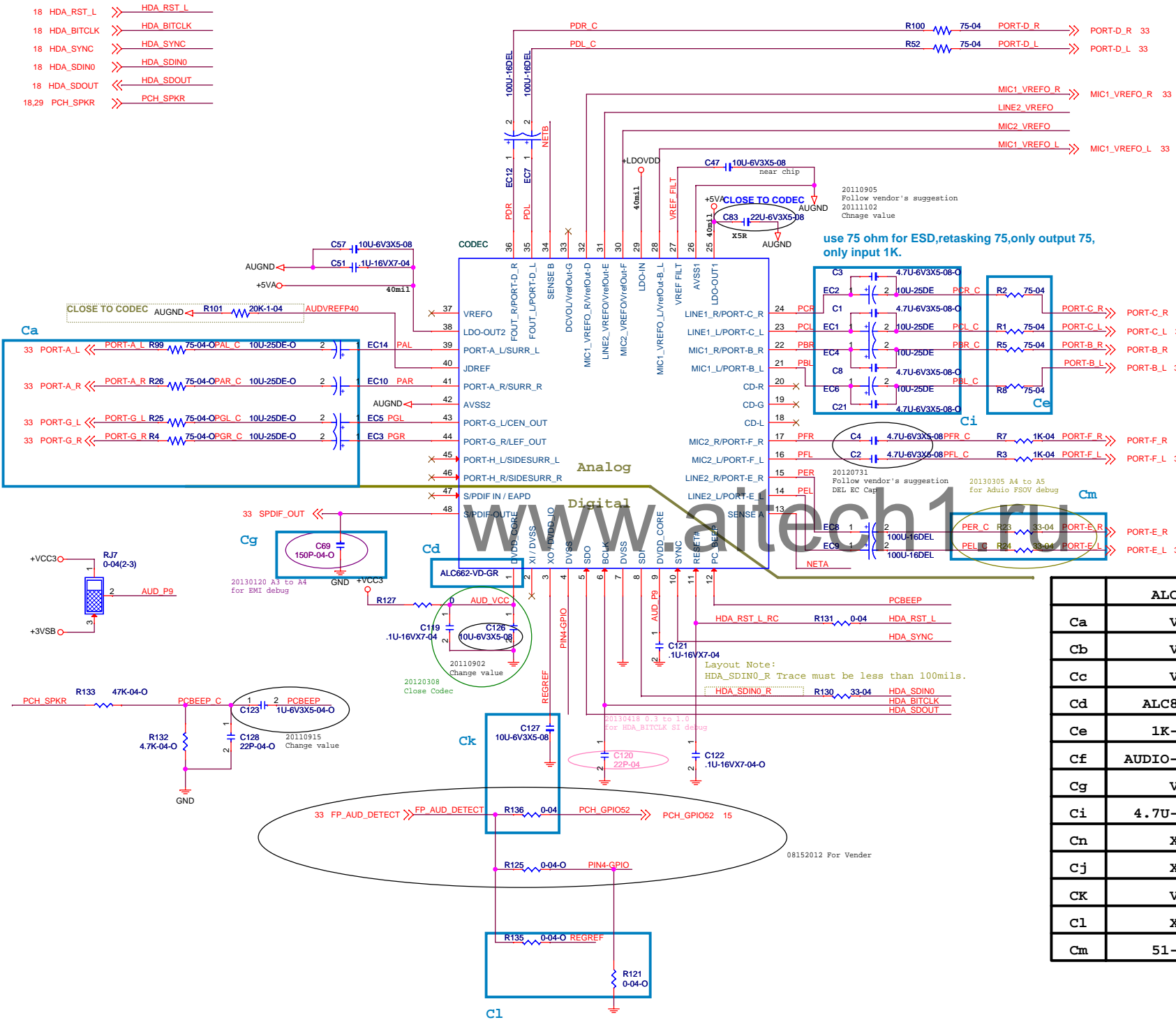
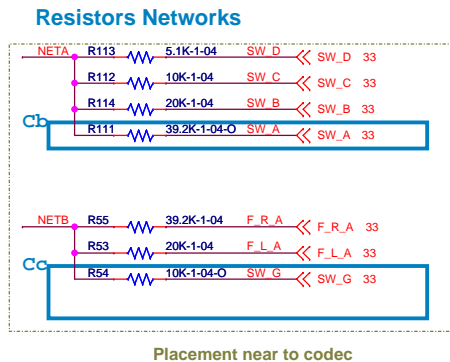
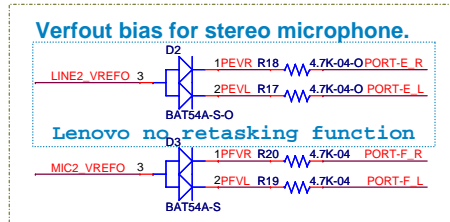
Place Caps in Bottom Side.

MDI0 P	SC4	2.7P-04-X-C
MDI0 N	SC1	2.7P-04-X-C
MDI1 P	SC5	2.7P-04-X-C
MDI1 N	SC3	2.7P-04-X-C
MDI2 P	SC16	2.7P-04-X-C
MDI2 N	SC14	2.7P-04-X-C
MDI3 P	SC18	2.7P-04-X-C
MDI3 N	SC17	2.7P-04-X-C

EMI value must be tuned?

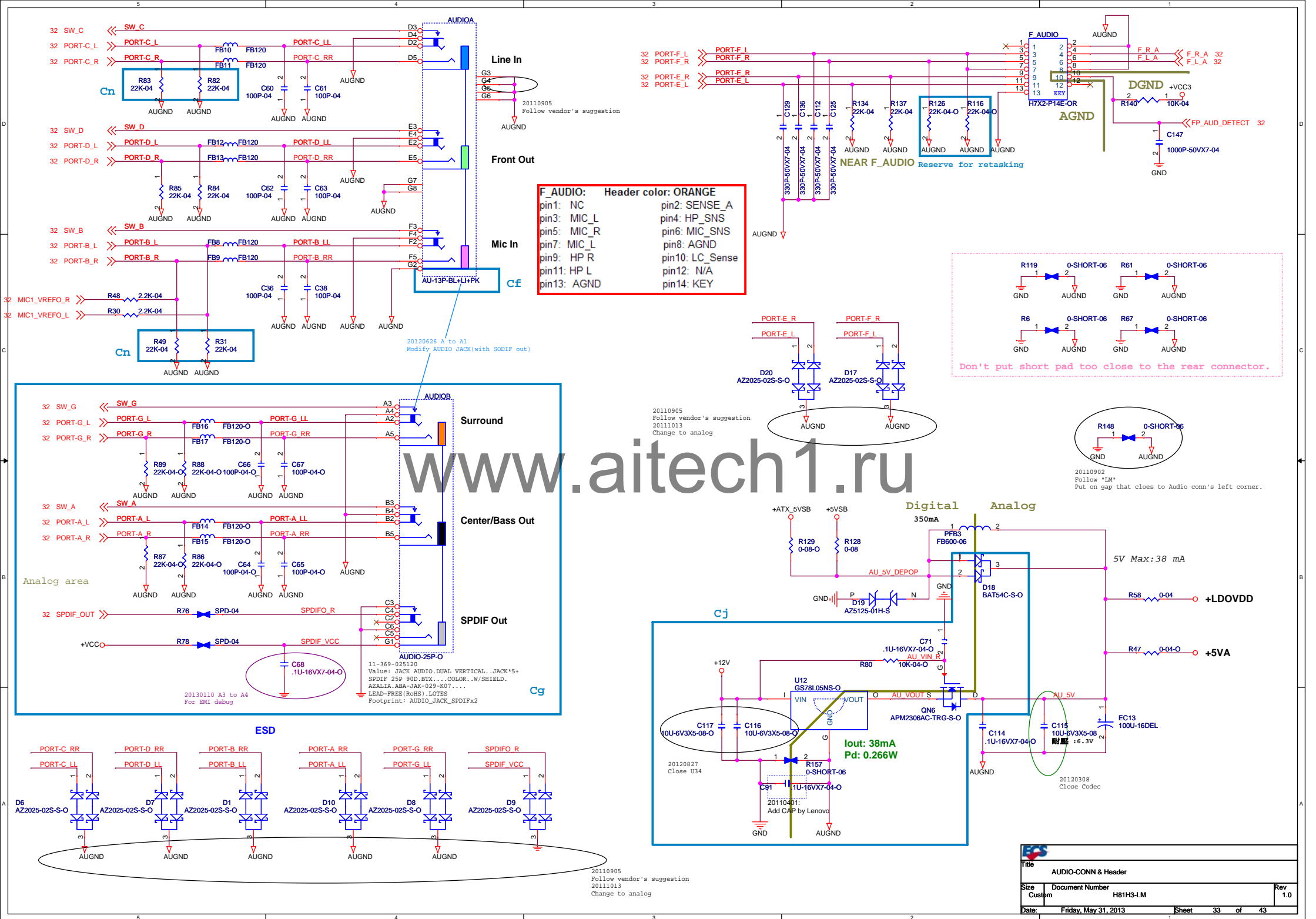


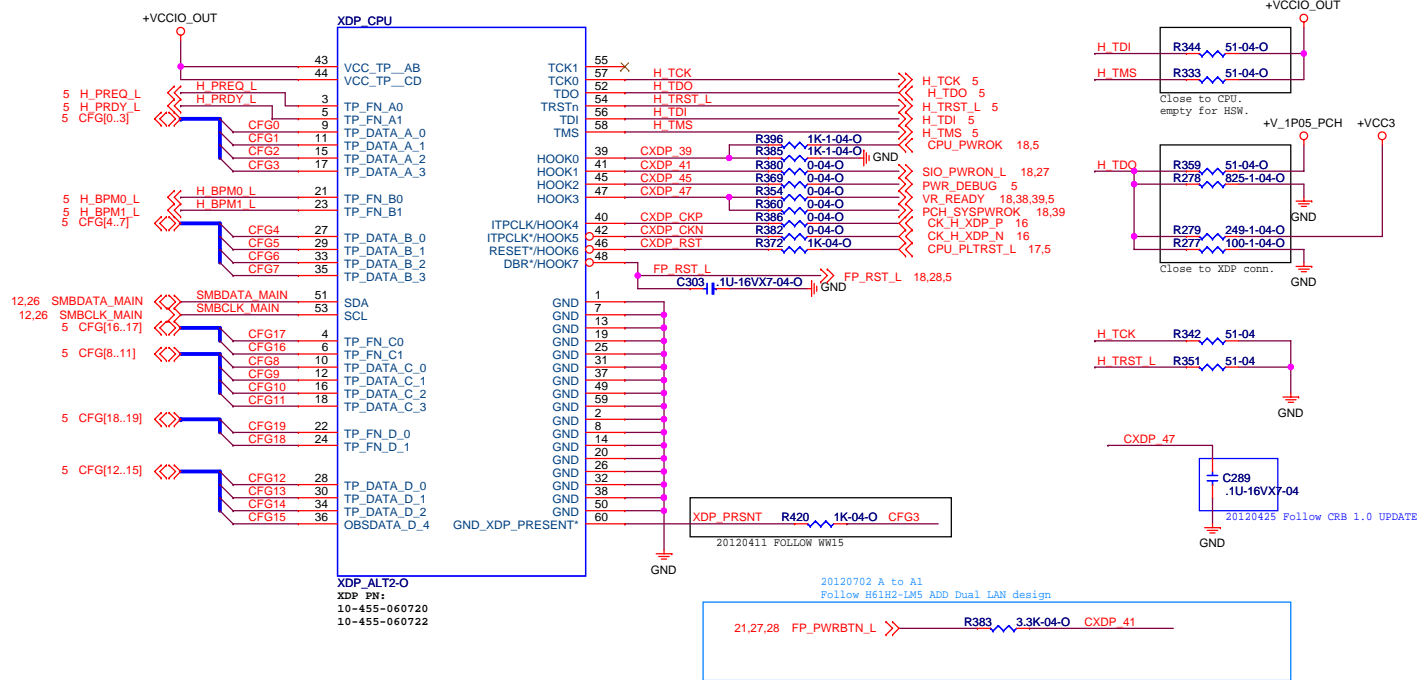
18 HDA_RST_L >> HDA_RST_L
 18 HDA_BITCLK >> HDA_BITCLK
 18 HDA_SYNC >> HDA_SYNC
 18 HDA_SDIN0 >> HDA_SDIN0
 18 HDA_SDOUT >> HDA_SDOUT
 18,29 PCH_SPKR >> PCH_SPKR



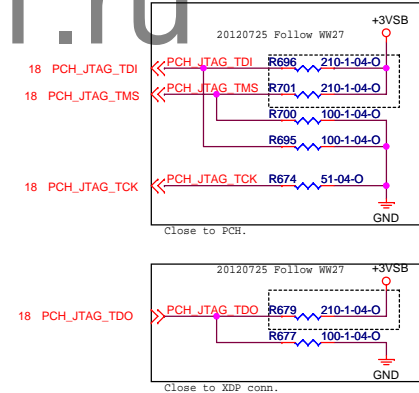
* default

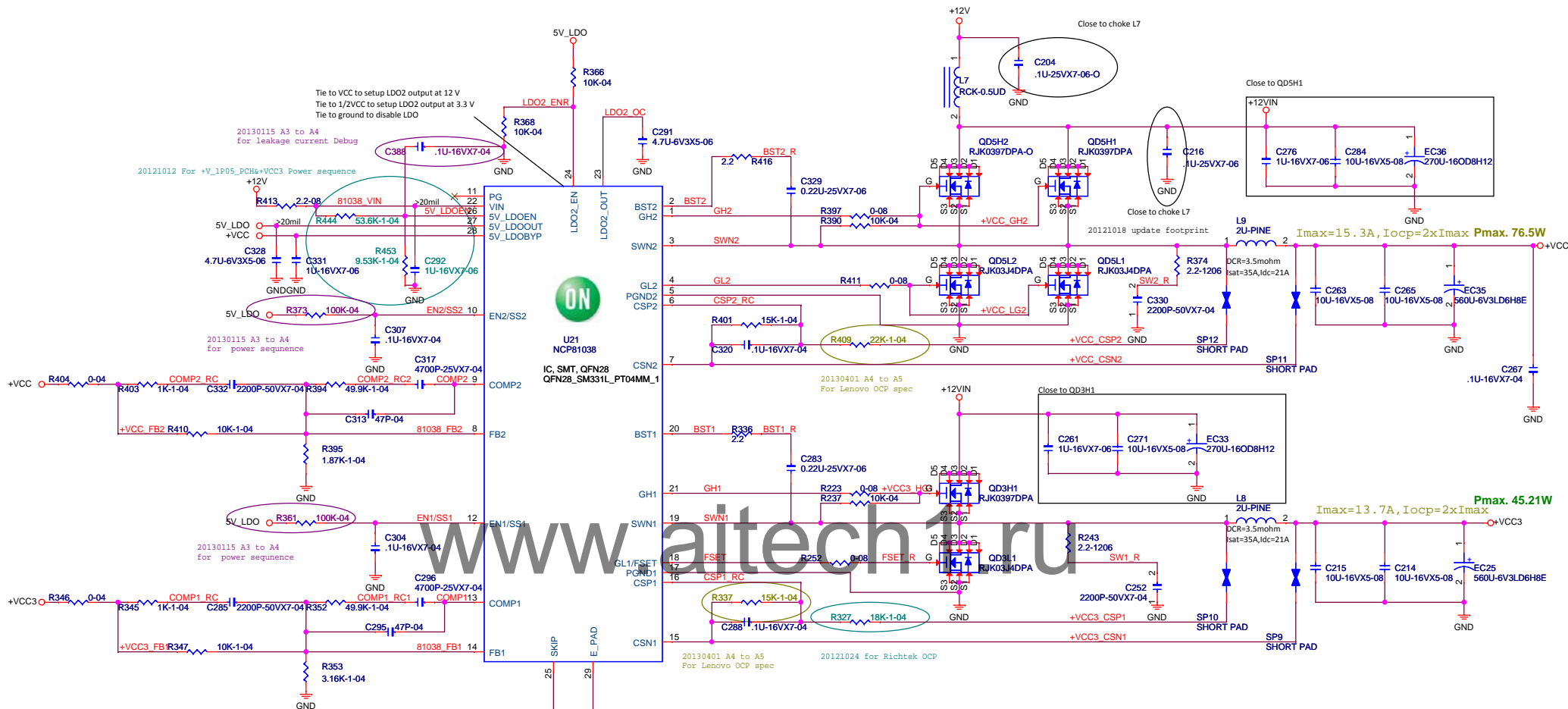
	ALC892	ALC662-VC	ALC662-VD
Ca	V	X	X
Cb	V	X	X
Cc	V	X	X
Cd	ALC892-CGS	ALC662-VC-GR	ALC662-VD-GR
Ce	1K-04	75-04	75-04
Cf	AUDIO-25P	AU-13P-BL+LI+PK	AU-13P-BL+LI+PK
Cg	V	X	X
Ci	4.7U-X5-09	10U-25D4H5E	10U-25D4H5E
Cn	X	V	V
Cj	X	V	X
CK	V	X	V
Cl	X	V	X
Cm	51-04	33-04	33-04





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DCM programming pin:
 1. Ground this pin to setup automatic CCM/DCM transfer with 33 KHz minimum switching frequency limitation;
 2. Connect this pin to VCC to force CCM operation;
 3. Leave this pin open to give automatic CCM/DCM transfer with 33 KHz minimum switching frequency for channel 1 but forced CCM for channel 2.

The R_{S1} , R_{S2} and C can be calculated as:

$$C \cdot (R_{S1} // R_{S2}) = \frac{1}{DCR}$$

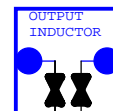
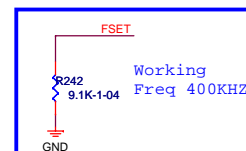
The inductor peak current limit is:

$$I_{LIM(Peak)} = \frac{V_{in,DC}}{k \cdot DCR} \text{ where } k = \frac{R_{S2}}{R_{S1} + R_{S2}}$$

The DC current limit is:

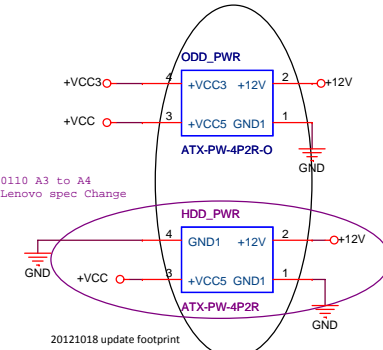
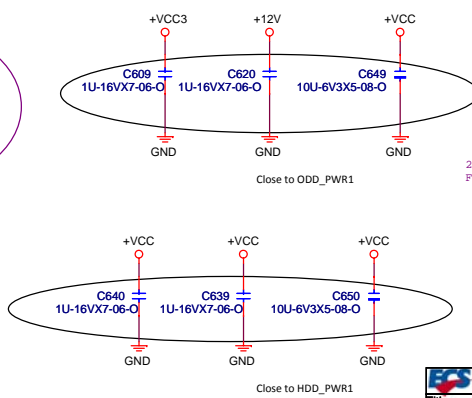
$$I_{LIM} = I_{LIM(Peak)} - \frac{V_{in} \cdot (V_{in} - V_{O})}{2 \cdot V_{in} \cdot f_{SW} \cdot L}$$

SPxx PLACE ON THE SOLDER SIDE, CLOSE INDUCTOR



BOM TO BOM IC :
 02-437-127790 IC PWM.RT8127GQW

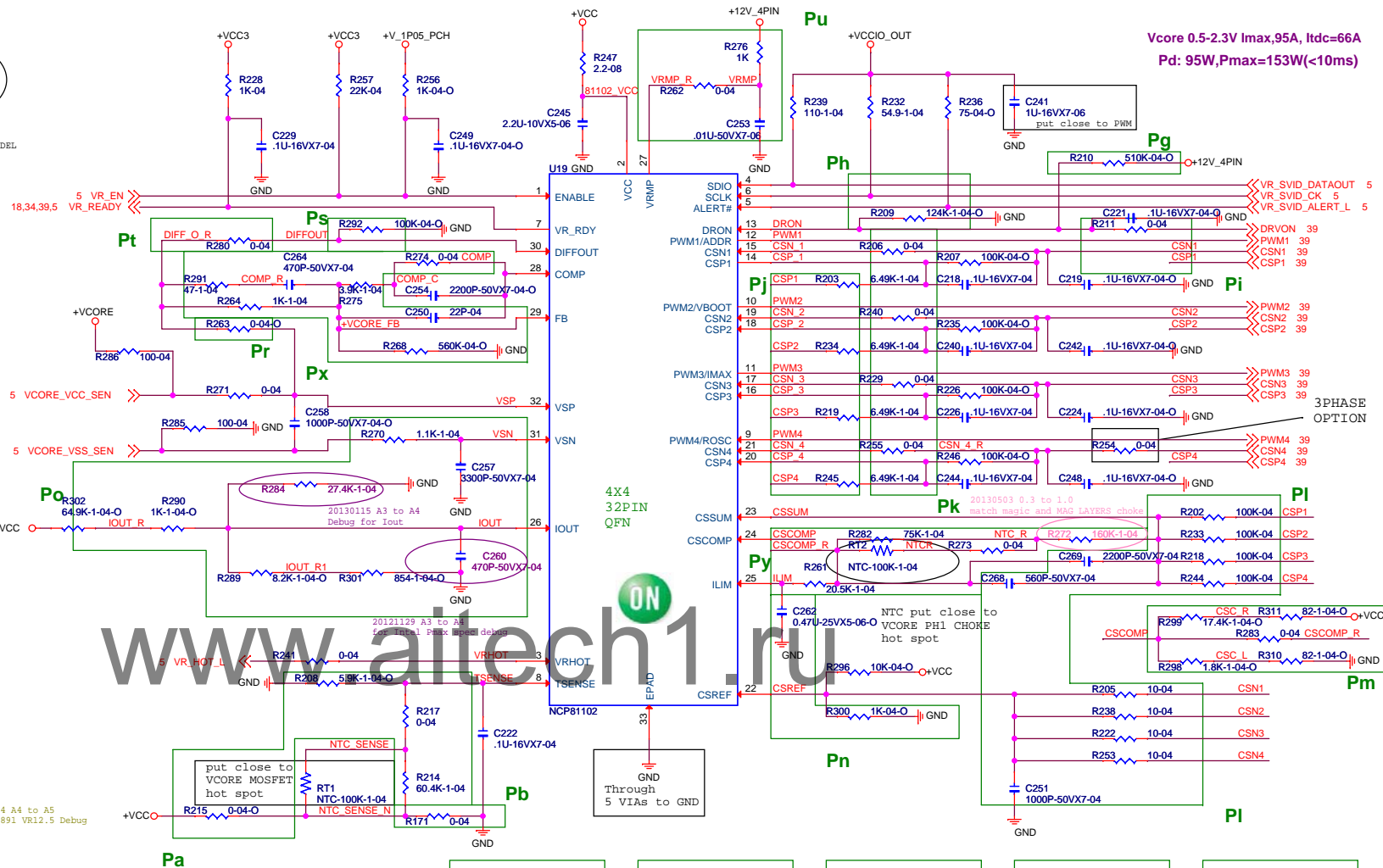
20130115 A3 to A4
 DEL R122



Title			
DC/DC VDIMM/DDR_VTT/5VDUAL			
Size	Document Number	Rev	
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	NCP81102+NCP81161	RT8891+RT9624D
Pa	R215=NC R214=60.4K-1-04 R208=NC R217=0-04	R215=0-04 R214=100K-1-04 R208=5.9K-1-04 R217=5.6K-1-04
Pb	V	X
Pc	V	X
Pd	V	X
Pe	V	X
Pf	V	X
Pg	X	V
Ph	X	V
Pi	V	X
Pj	6.49K-1-04	5.1K-1-04
Pk	0-1-04	680-1-04
Pl	V	X
Pm	R283=0-04 R311=NC R310=NC R299=NC R298=NC	R283=NC R311=82-1-04 R310=82-1-04 R299=17.4K-1-04 R298=1.8K-1-04
Pn	X	V
Po	R302=NC R284=27.4K-1-04 R290=NC R289=NC R301=NC R270=1.1K-1-04 C260=470P-50VX7-04 C257=3300P-50VX7-04	R302=64.9K-1-04 R284=NC R290=1K-1-04 R289=8.2K-1-04 R301=845-1-04 C260=NC R270=0-04 C257=NC
Pr	X	V
Ps	X	V
Pt	V	X
Pu	R276=1K R262=0-04 C253=.01U-50VX7-06	R276=1 ohm R262=130K-04 C253=2.2U-16VX5-06
Px	R264=1K-1-04 R291=47-1-04 R274=0-04 R275=3.9K-1-04 C250=22P-04 C264=470P-50VX7-04	R264=10K-1-04 R291=0-04 R274=51.1K-1-04 R275=3K-1-04 C250=100P-04 C264=220P-50VX7-04
Py	R272=150K-1-04 R282=75K-1-04 R273=0-04 R261=20.5K-1-04	R272=3.32K-1-04 R282=12K-1-04 R273=15.8K-2-04 R261=0-04

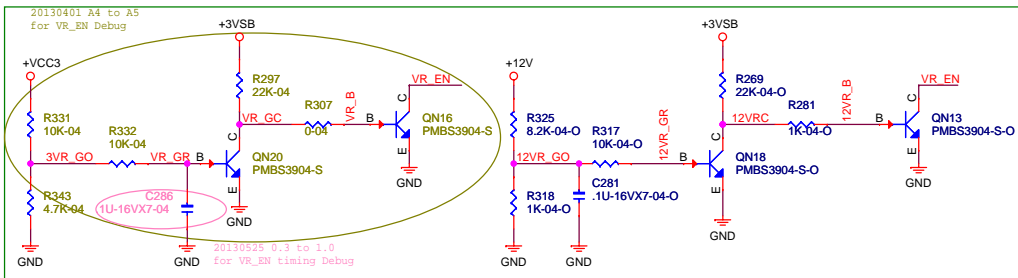
20120809 DEL



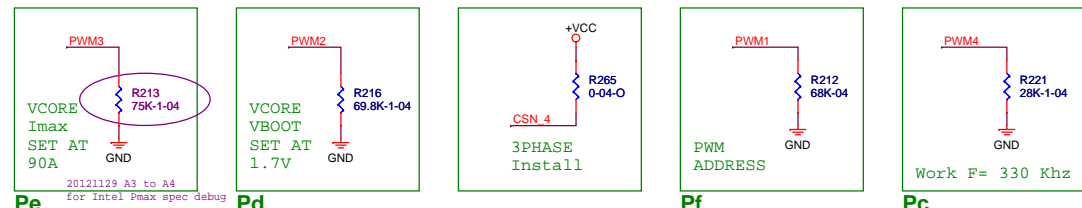
20130314 A4 to A5
for RT8891 VR12.5 Debug

20121015 Change Vaule for Vore test debug

20121129 A3 to A4
for Intel Pmax spec debug



VRM Sequencing Circuit

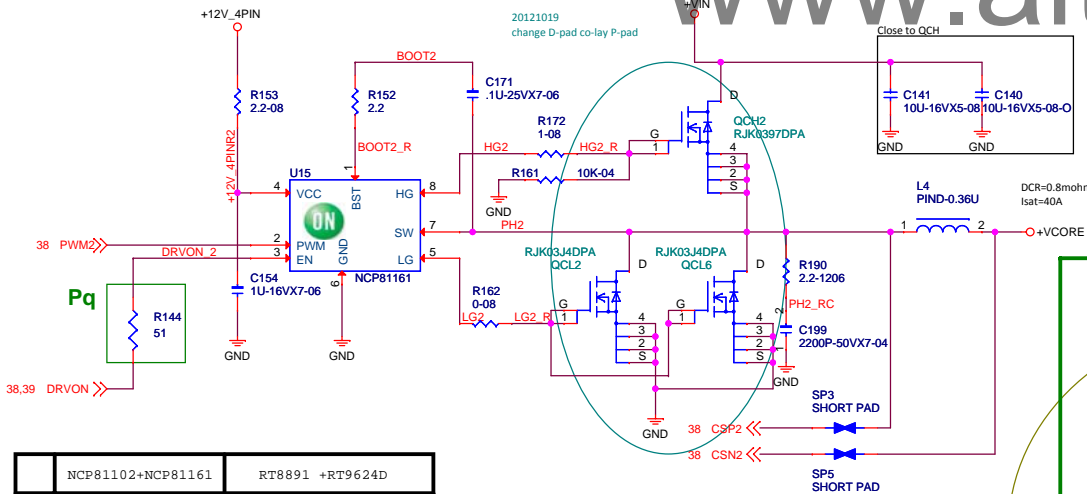
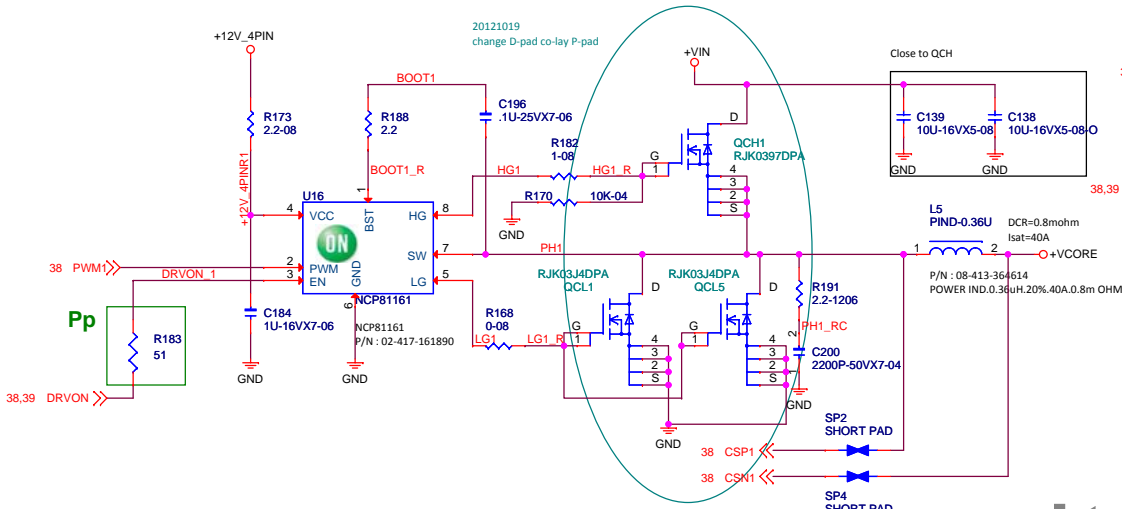
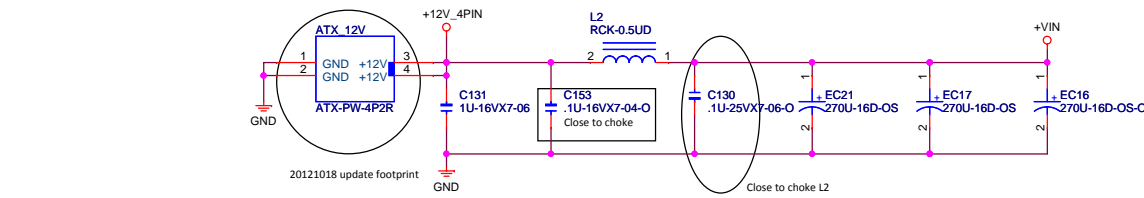


Programming ICC_MAX

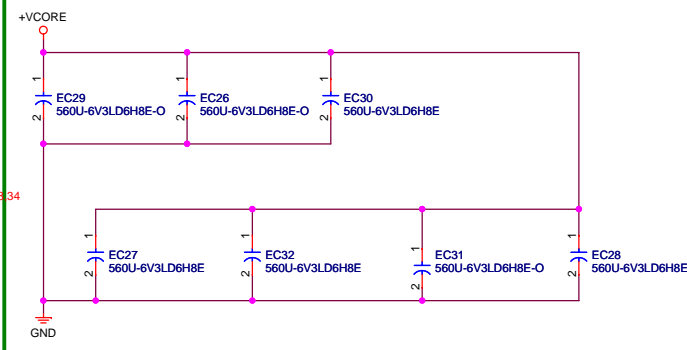
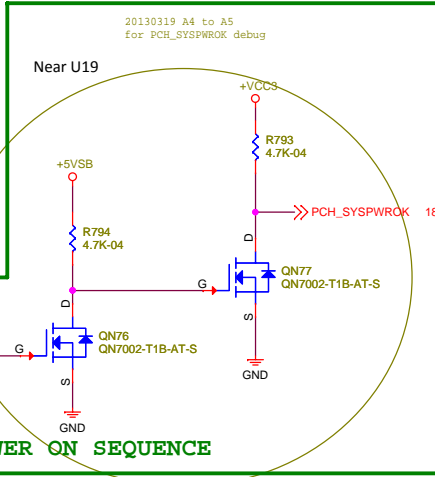
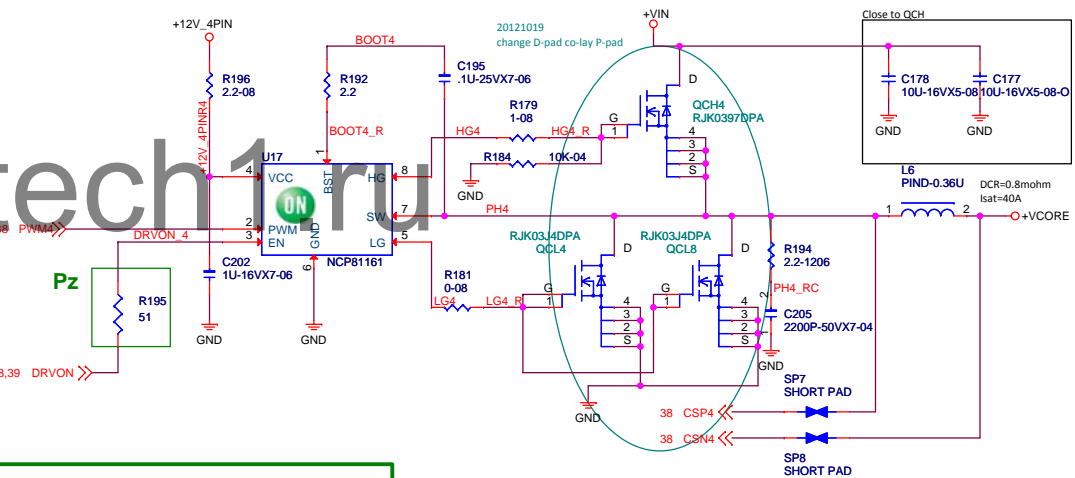
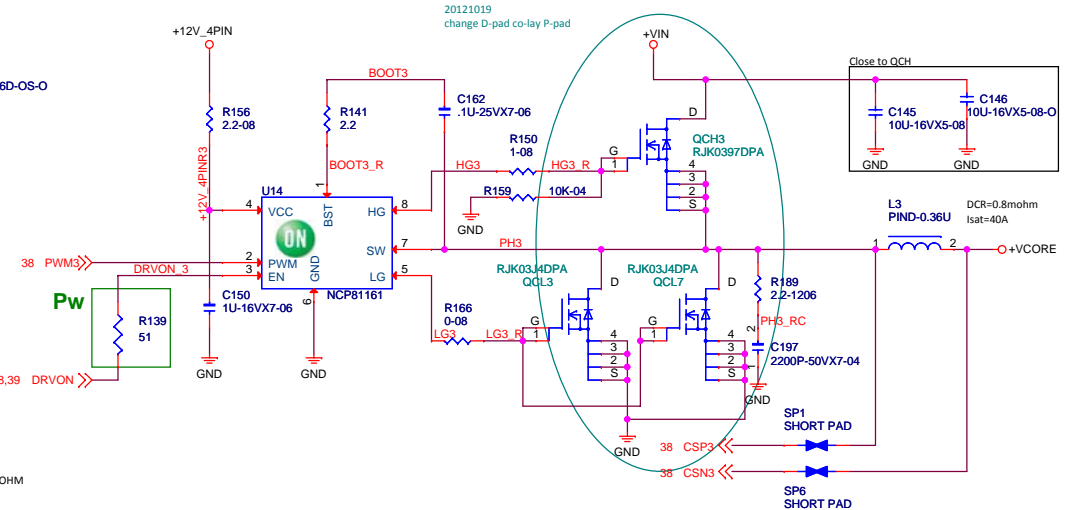
The SVID interface provides the platform ICC_MAX value at register 21h for. A resistor to ground on the IMAX pin programs these registers at the time the part is enabled. 10uA is sourced from these pins to generate a voltage on the program resistor. The value of the register is 1A per LSB and is set by the equation below. The resistor value should be no less than 10K.

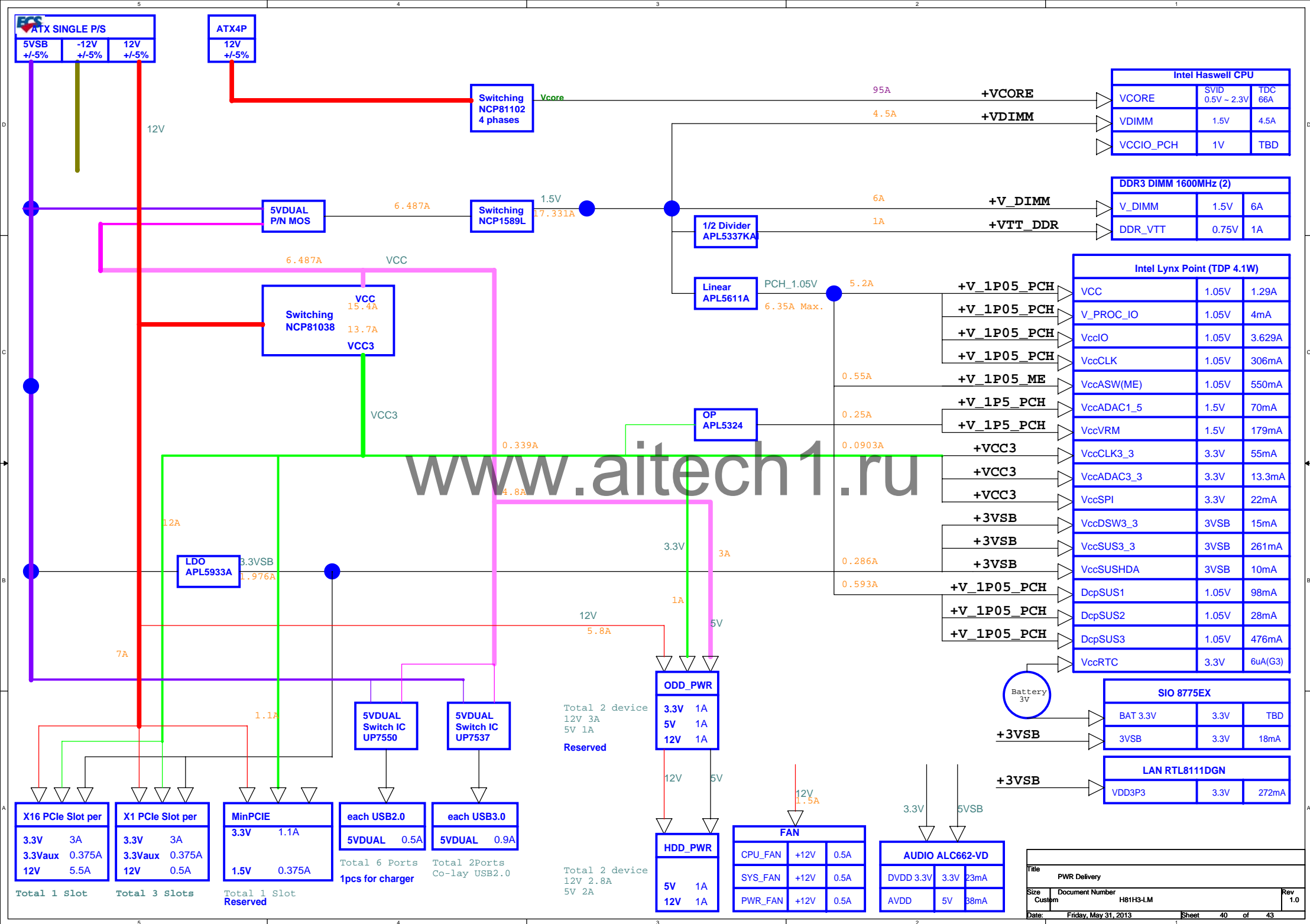
$$ICC_MAX_{21h} = \frac{R * 10\mu A * 256A}{2V}$$

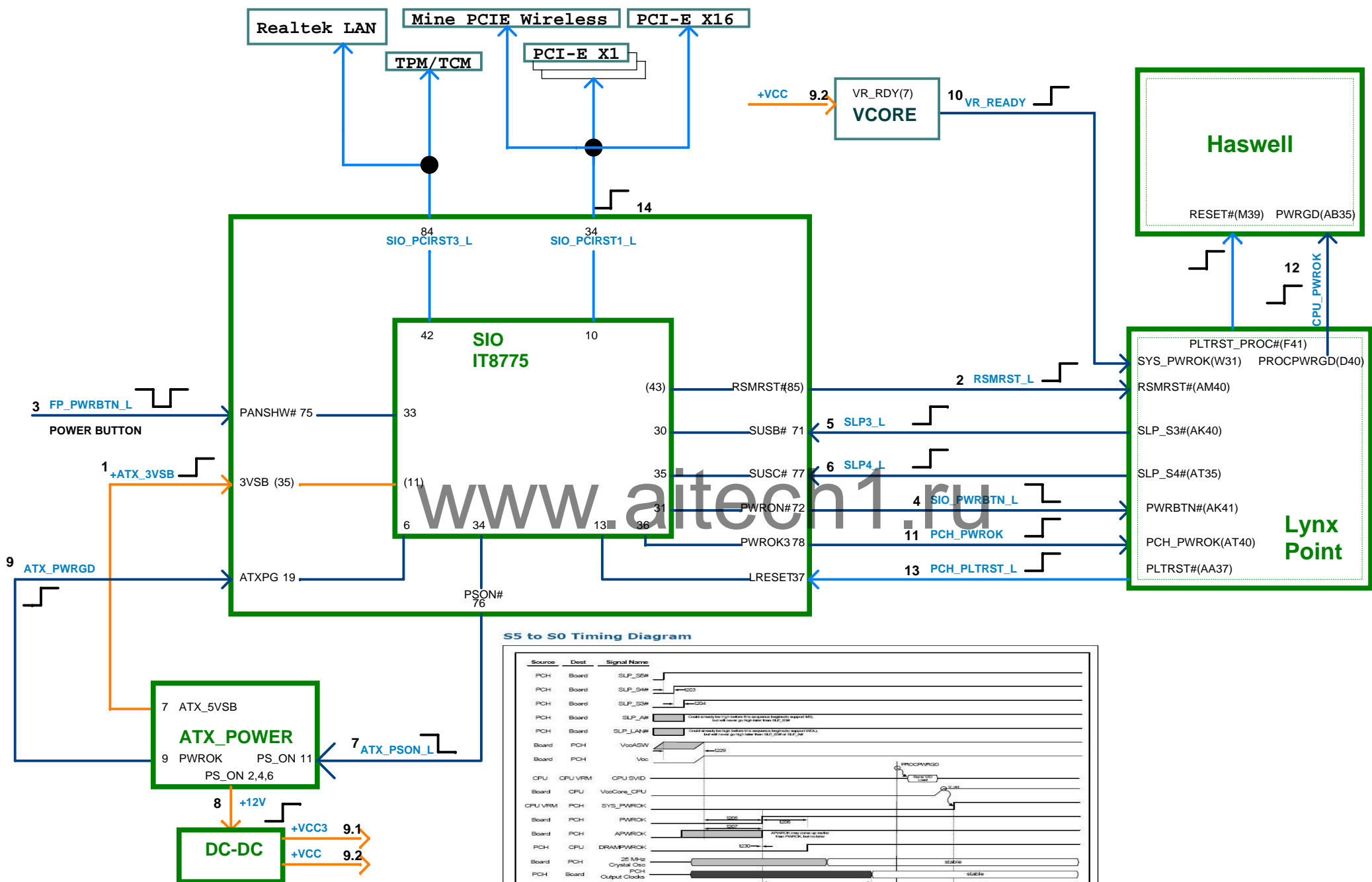
Title			DC/DC Vcore_Controller
Size	Document Number	H81H3-LM	
Custom			
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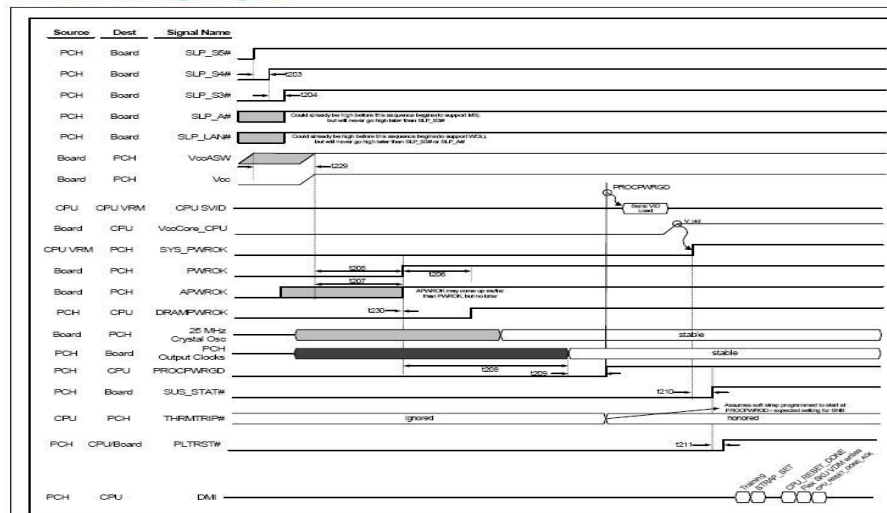
	NCP81102+NCP81161	RT8891 +RT9624D
Pq	V	X
Pp	V	X
Pw	V	X
Pz	V	X

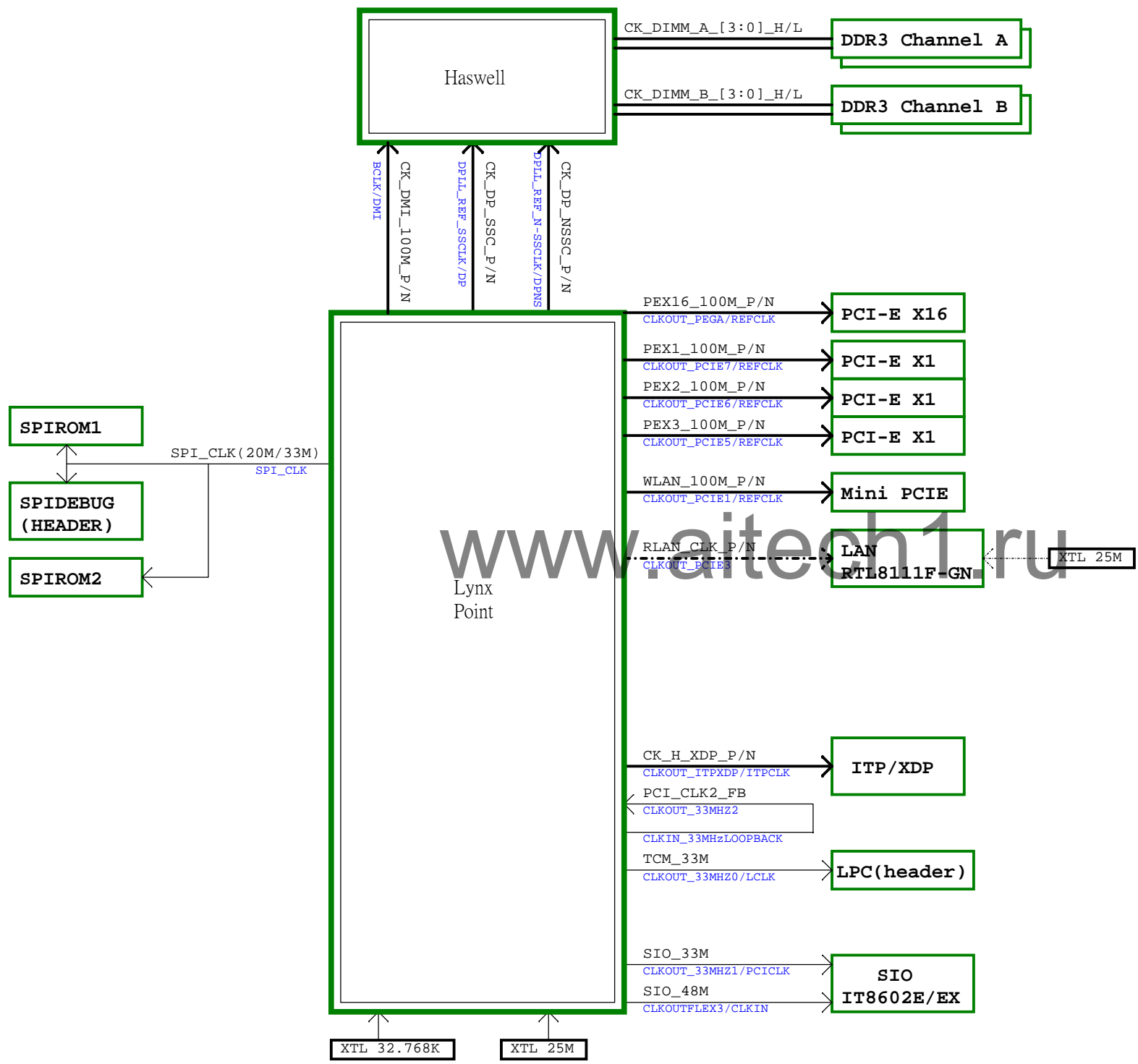






S5 to S0 Timing Diagram





REVISION HISTORY:

Rev	Date	Notes
A2	2012/08/16	From H81H3-LM V:A


Rev	Date	Notes
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A3	2012/09/30	1. U33 From APL5932AKAI Change to APL5933AKAI for Vender Process 2. DP Dongle Detect circuit form +VCC change to +12V 3. QN66,QN67 from 3904 chage to 2N7002 For Dongle Detect debug 4. R348 Resrve for Intel no Overclocking function 5. Del HSW Strap CFG13 circut H81 no Overclocking function 6. R272 Change Vaule for Load Line debug 7. R284 Change Vaule for lout Debug 8. USB3.0 TX Signal Option Swap for Layout 9. ATX_POWER change footprint for Lenovo IPG V2.1 spec 10. ME_DIS control circuit reserve For Lenovo Require 11. RJ16 DEL for BOM detect is enough 12. ADD R530,R660,R661 For USB OC function Debug 13. ADD R406 for reboot Issue from Intel WW39 14. TPS2543 Control Mode chahge for Lenovo spec 15. Vore option Table(RT8891+RT9624D) change Vaule for test debug 16. ADD DP function for Lenovo spec 17. ADD DPWROK cirtcuit for Intel Timing(Deep Sx to G3) 18. QCH1,QCH2,QCH3,QCH4,QCL1,QCL2,QCL3,QCL4,QCL5,QCL6,QCL7,QCL8 change D-pad co-lay P-pad for Lenovo require 19. Reserve C316 for MIN_PCIE USB signal stitching cap 20. R90 Change 0603 to 0805 for Lenovo IPG 21. Y HOLDER1 change to Iron wire for Lenovo require 22. Reserve C662,C663,C664,C665 for EMI debug 23. R409,R327 from 21K change 18K to for +VCC&VCC3 OCP debug 24. DEL USB Charger Power-On Reset circuit for Lenovo require 25. Update USB Charger circuit for Lenovo require 26. DEL R224 for USB OC_3 debug 27. Power circuit(+USBVCC6) from UP7550 change to DUAL MOS(APM4500AKC) for Lenovo require 28. F_USB2 USB port(USB +/-10) power from +USB_CHARGER1 change to +USBVCC6 29.Reserve Stitching cap C273,C278 for USB3.0 Slot 30.F_USB2 of USB port 10 and 11 SWAP for Lenovo require 31.PCIE WAKE Mode change for WOL G3 to S5 function 32.ADD R444,R453 For Intel +V_1P05_PCH&+VCC3 Power sequence 33. DEL EC34, ADD C390 for layout space 34. C670,C666,C693,C672,C668,C667 Reserve for SPI Debug 35. DEL PCH XDP Header for Lenovo Require 36. Reserve C394 for +DIMM_5VDUAL noise debug Lenovo Require 37. Reserve EC55 for +5VSB noise debug Lenovo Require 38. Reserve C669 for 48M Clock debug 39. ADD R324,C671 to USB_EN1 delay for Lenovo Require 40. QN9,QN10,QN39,QN55,QN32 from 3490 change to 2N7002 for Lenovo Require 41. ADD +VDIMM circuit(1.5V coly-lay 1.35V) for Lenovo Require 42. +V_1P5_MINI power circuit change to LDO for Lenovo Require 43. ADD F3 for +VDD3 timing spec 44. ADD QN78,Q2 for OBFF debug
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Rev	Date	Notes
0.2	2013/01/18	1 .SIO form IT8775EX change to IT8612E/CX co-lay IT8612E/DX for spec change 2. DEL SSD_PWR circuit for spec change 3. Resrve R72 follow CRB 4. DEL C16,C14,C15 for VGA Rise and Fail time debug 5. C25,C26,C27 change to 10pF for VGA Rise and Fail time debug 6. R79 change to 3K,ADD RJ6(1-2),RJ4(1-2) For HDMI Debug 7. DEL SPIROM2 circuit for Lenovo Spec change 8. DEL Case Open circuit for Lenovo Spec change 9. USB_OC3_L pull-high change to +3VSB For MINI_PCIE Compatibility debug 10.DEL R398,R391,R367,R376 for For SSC_DPLL_REF_CLK and DPLL_REF_CLK debug 11. Reserve R72 to GND follow CRB Resrve 12. EC51 from 220uF change to 470uF for Lenovo Spec 13. ADD +USBVCC_SW3 of USB Discharge Circuit for Lenovo Spec 14. +V_3P3_MINI,USB Charger power,+USBVCC6 Circuit change for Lenovo require 15. U23 from APL5317 change to APL5611 for Inrush Current debug

0.3	2013/03/25	1 .R23,R24 change to 33 ohm for Audio FSOV Debug 2. R454 change to 0 ohm Follow WW9 PDG2.0 update 3. RJ21(2-3),RJ22(1-2),RJ23(2-3),RJ24(2-3) change to 0 ohm For Power LED debug 4. C581 change to 33pF for SLP_S3 debug 5. USBLAN change to Solid-state semiconductor For Lenovo spec 6. BOSS1,BOSS2 change to M2.0 For Lenovo spec 7. ADD C648,C160(2700pf) For Thermal debug 8. DEL R293,R305 For SIO change to 8602E/DX 9. ADD VR_READY POWER ON SEQUENCE Circuit For PCH_SYSPWROK Debug
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1.0	2013/05/23	1. R272 from 150K change to 160K for match magic and MAG LAYERS choke(P.38) 2. RJ19 change to (2-3) For PWR_FAN function(P.18) 3. ADD R293,R305 RJ23,RJ24 change to (1-2) for PWR_FAN Function(P.27) 4. ADD C485(22uF) and EC37 For After Power loss debug(P.29) 5. Resrve R295 for Intel MOW 15 not support 2014 CPU(P.5) 6. Resrve SC19,SC20,SR12,SR15,SR14 For Intel MOW 15 not support 2014 CPU (P.7and P.8) 7. C100 (10uF) For Lenovo spec For VDD33 power noise debug(P.30) 8. RJ12 from (2-3) change to (1-2) for SIO form 8602DX change to 8602EX BOM selection(P.15) 9. R471 from 39 change to 47 ohm for SIO48M Monotonic debug(P.16) 10.R500 from 33 chnge to 51 ohm for HDA_BITCLK Monotonic debug(P.17) 11.ADD R314 (1K) For V_3P3_MINI Discharge debug(P.22) 12.Resrve R544 and R231,add R550(10K) Reserve For Lenovo spec require(P.22) 13.ADD R665 and R334, Resrve R467 for USBVCC_SW Drop debug(P.23) 14.RJ21 from (1-2) change to (2-3) ,RJ22 from (2-3) change to (1-2) for SIO from 8602DX change to 8602EX(P.27) 15.RJ23,RJ24 from (2-3) change to (1-2) PWR_FAN for Lenovo change to COM2(P.27) 16.ADD C518(10u) ,R609 from 300K change to 0 ohm, DEL C546,R610 from 0 change to 100K,R628 from 0 change to 300K,ADD C564(0.01uF)(P.37) 17. ADD C286(0.1uF)20130525 0.3 to 1.0 for VR_EN timing Debug (P.38)
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